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Novel pseudo PMOS ultraviolet photo catalytic oxidation (PP-UVPCO) sensor for air purification

Abstract

The paper presents a performance analysis of Novel CMOS Integrated Pseudo PMOS UVPCO having zero static power dissipation. The main emphasis is on simulation of power and performance analysis along with the comparison with existing devices, which is used for Air Purification. This approach can improve calibration without the use of a high speed digital processor. The conventional devices consume high power and are not firm for long term monitoring. These devices are also suffered from low value of slew rate, high power consumption, and non linear characteristics but in this novel design the device has almost zero static power, less load capacitance on input signals, faster switching, fewer transistors, higher circuit density and the device has better slew rate. This device has a modest architecture, and suitable for Air purification and surface sanitisation.

Index Terms-ultra violet photo catalytic oxidation (UVPCO), air purification, slew rate, SPICE, surface sanitization.

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Introduction

Nowaday's air pollution is increasing because of harmful material in earth atmosphere causing deceases, deaths, and damage to crop. These harmful material can be natural origin or man-made. The main source of these harmful materials is power plant and manufacturing factories. The main air pollutant which can have adverse effects on humans and the ecosystem, are sulphur oxide, carbon monoxide, volatile organic compound, chlorofluorocarbons ammonia and toxic metals. These air pollutants can have adverse effect on human health like headache, fatigue, poor memory, respiratory irritation, pneumonia in children, lung cancer, heart disease, eye, and nose and throat irritation.

Hence, there is a need to purify air by using advanced process called Photo Catalytic Oxidation (PCO). In PCO Titanium dioxide is used as a catalyst which cleans the air.[1–3] As air falls on this catalyst, electron will get energy and released at its surface. Then it will interact with water molecules in the air, as we know that electron having energy which breaks the water molecules into hydroxy1 radicals, hydroxide and hydrogen peroxide.[4] These hydroxy1 radicals are more reactive so they attack organic pollutant molecules, breaking them into carbon dioxide and water which are harmless substance. The methods used for photo catalytic oxidation applications includes massive set ups and require ample time for computation and complex calculations. The complete photo catalytic oxidation process is shown in Figure 1.[5,6] This process is responsible for purify air up to significant level, to measure that level there is a serious need of sensor which tell the percentage purification of air. Novel CMOS Integrated Pseudo PMOS UVPCO (PP-UVPCO) model having zero static power dissipation is presented in this research studies which gives an air and surface sanitization readings.[7–9]

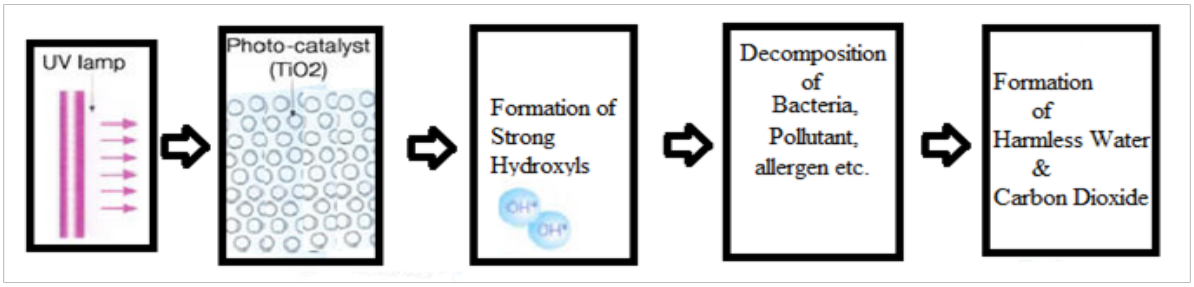

Figure 1 Process of photo catalytic oxidation.

Now a days due to multipurpose demands i.e all the things on a single chip, complex functions are built. To realize the complex function on the same chip there is growing demand for high density VLSI circuits. One of the practical solutions is to scaling of transistor and Vdd. The major problem which effect is an exponential increase of leakage or static power in deep sub-micron technology. Hence to overcome this problem a portable device for air quality monitoring applications is highly desirable. With the advancement in technology, the channel length of the transistor decreases (i.e Technology) this leads to increase in the transistors density per unit chip area, due to scaling of the device and very large integration of the transistors will lead to increase in temperature and higher power consumption inside the device.[10–12]

The increase in temperature will lead to the increase in the overall cooling cost which further impact the necessary packaging techniques cost. Power plays an important role for selecting any digital device. One of the important parameter on which total power consumption in the modern digital circuits depends is leakage currents. Leakage power contributes to 39.9% (approx) of the total power consumption in the modern high performance monitoring circuits.[13–16] Hence, It

is necessary to work on reduction of leakage current which intern reduces the leakage power and thus useful for a modern digital low power design. The relationship between leakage current and leakage power dissipation is given by (1).

$$P_{static} = I_{leak} * V_{dd} \quad (1)$$

Where,

I_{leak} indicates the leakage current when the device is in OFF state

V_{dd} is the supply voltage.

Leakage current is mainly depends on the following factors

a. Gate leakage

b. Sub threshold leakage

c. Reverse-biased junction leakage

d. Gate-induced drain leakage

From the all above factors it is found that the major components which affect the leakage power are sub-threshold leakage and gate-leakage. The relationship of sub threshold leakage current is shown in (2)

$$I_{sub} = I_0 exp\left[\left(V_{gs} - V_t\right)/\left(nV_T\right)\right]\left[-exp\left(-V_{ds}/V_T\right)\right] \quad (2)$$

$$I_0 = \mu_{eff} C_{ox} \left(W/L\right) V_T^2 \quad (3)$$

Where,

W and L are channel length and width

Vt is the threshold voltage

μeff is the electron/hole mobility

Cox is the gate oxide capacitance per unit area

n is the sub-threshold swing co-efficient

V_T is the thermal voltage

V_{gs} is the transistor gate to source voltage and

V_{ds} is the drain to source voltage.

PCS macro model

Photo Catalytic Sensor is a MOSFET in which the gate terminal is floating and connected with chip in the form of reference electrode placed in an aqueous solution.[17–19] The current-voltage relationship in active mode for PCS is same as that of MOSFET as given below in eq.4.

$$Ids = C_{ox}\mu W / L[(V_{gs} - V_t)V_{ds} - 1/2V_{ds}^2] \quad (4)$$

Where,

Cox is the oxide capacitance per unit area,

μ is the electron mobility in the channel,

W and L are width and the length of the channel respectively.

In the above relationship shown in the equation 4 if all other parameters like β, V_{ds} and V_t are taken constant Ids is depends upon on V_{gs} only. The relationship of threshold voltage with others parameters is given below in eq. 5.

$$V_t = \frac{\phi_M - \phi_{si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \quad (5)$$

Where,

ϕ_M : Work function of gate metal.

ϕ_{si} : Work function of silicon gate.

Qox: Oxide charge.

Qss: Interface charge carriers.

QB: Depletion charge carriers.

The fabrication steps for PCS and MOSFET are same due to which the threshold voltage equation of PCS looks a lot like with that of MOSFET. The equation included all necessary parameters as that is used in the formation of MOSFET equation. Although the concept of forming the equation is same but there are two additional following terms are also added.

(1) Constant reference electrode potential Eref.

(2) Interfacial potential which consists of chemical input parameter (Ψ) which depends on concentration of O2 in the solution and surface dipole potential (χsol).

The above mentioned two parameters along with eq. 5 helps in the formation of threshold voltage equation for photo catalytic sensor and shown below in eq. 6.

$$V_{th\,(PCS)} = E_{Ref} - \Psi_{air} + \chi^{air} + \frac{-\phi_s}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \quad (6)$$

As the characteristics of the MOSFET gate to source voltage the input gate to source voltage Vgs and the drain current I_d is indorsed to vary with drain to source voltage while the reference voltage E_{ref} kept constant. The eq. 6 has been modified such that Ψair is taken as a function of O_2 concentration in place of a function of pH as given by Grattarola et al.

On Comparing PCS with MOSFET keeping the concentration of O2=1mg/l constant, it is observed that the characteristic resembles with MOSFET keeping gate to source voltage constant as shown in Figure 2. At Vref.=0 V it is observed that for different concentration levels of Oxygen, different Characteristics curves are obtained. From the above it is concluded that Photo Catalytic Sensor can be treated as MOSFET on the basis that the chemical input parameter Ψsol is a function of O2 (Ψsol=f (Oxygen)).

The Modern analog building block used for designing current mode devices are Current Conveyor (CC-II) (Figure 3) introduced by Sedra and Smith.[17–20] CC has many application ranging from low power signal processing to implement of numerous analog processing applications. The Matrix relationship between input output current and voltage is shown below. The general CC can be expressed by the following input-output matrix relation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

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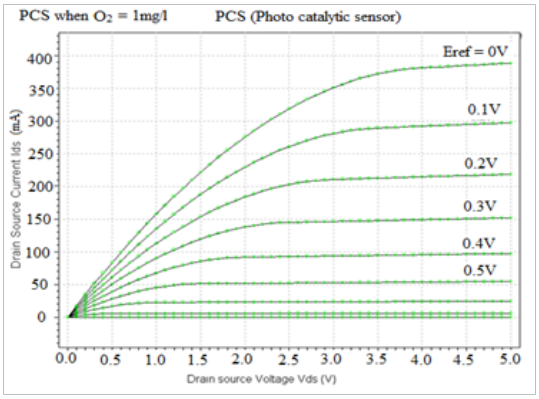

Figure 2 Simulation result of PCS as MOSFET.

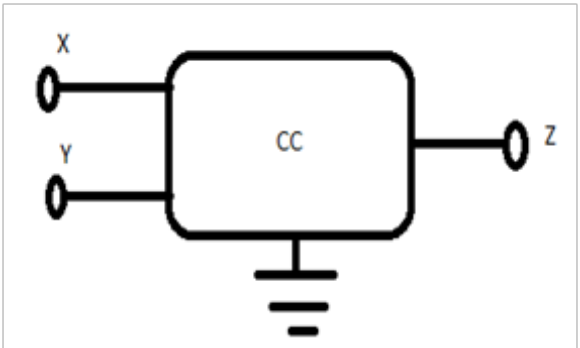

Figure 3 Block diagram current conveyor.

Different values of a and b leads to different functionality of the CC as follow

a. When value of a=1, the first generation current conveyor (CCI) is obtained.

b. At a=0, we obtain the second generation current conveyor (commonly denoted CCII).

c. With a=-1 we obtain the third generation current conveyor (commonly denoted CCIII).

d. Usually, b=±1. The sign of the b parameter determines the conveyor current transfer polarity.

e. For b=1 indicates that the CC has a positive current transfer ratio and is denoted by CCI+, CCII+ or CCIII+ while with negative b means that it has a negative current transfer ratio and is denoted by CCI-, CCII-or CCIII-

f. Form the all above discussed generation the second generation current conveyor (CCII) is most commonly used. An important attribute of current conveyor is its ability to convey current between two terminals (X and Z) at vastly different impedance levels as represented by the matrix.

Pseusedo-NMOS

logicPseudo-NMOS technique is based on ratioed logic in which a grounded PMOS is used as a Pull up. The NMOS driver circuit is used as pull-down network that realizes the logic function. The main advantage of this logic is it uses only N+1transistors as compared to 2N transistors for CMOS logic. The CMOS logic has less load. Capacitance on input signals, faster switching but have higher circuit density. In Pseudo-NMOS logic the high output voltage level for any gate is Vdd and the low output voltage level is not zero volts.[20–25] The only main drawback of this logic is very high static power consumption which is not zero and exists because there is direct path between Vdd and ground. The size of PMOS device must be kept smaller than NMOS pull-down devices for making it low power. To increase the speed particularly when driving many other gates the PMOS transistor size has been increased. Therefore there is always a trade-off between the parameters noise margin, static power dissipation and propagation delay.

Device description and analysis

For the integrated sensor, the measurement circuit tracks the threshold voltage of the PCS which is varied as the concentration of O2 is varied. One of the solution to resolve the high power consumption problem by add-on sensor network is to integrate the sensor with electronics as a circuit component in an integrated circuit rather than as an add-on sensor whose output signals is further processed. In this research studies, the PCS is used as one of the input transistors in the differential stage of the current conveyor as shown in Figure 4. The function of the circuit is described as follows: In this circuit the PCS-Current Conveyor is configured as a voltage follower. In the voltage follower circuit the output voltage (Vo) is equal to the input voltage (Vin). This circuit is so sensitive that any difference in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output.

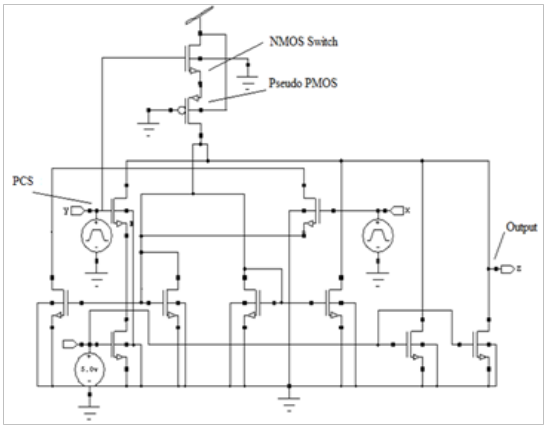

Figure 4 Circuit diagram of pseudo PMOS UVPCO.

The well-known distinct advantages of Pseudo PMOS like less load capacitance on input signals, faster switching due to fewer transistors and higher circuit density encourages us to implement this novel design. The only disadvantage of this logic is that the circuit is always on due to which there is significant static power dissipation which is a serious drawback. There are several methods to reduce the static power dissipation but there is no method so far technologically advanced to completely avoid this drawback. In this novel design the circuit has almost nil static power dissipation.

The circuit given below is designed using Pseudo PMOS technology in which gate of PMOS is grounded. There is one NMOS just above the grounded PMOS which act as a switch and ON only when the input is applied. As the circuit is ON along with the input signal hence there is no direct path from V_{dd} to ground which prevent the circuit from the static power dissipation.

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Timing analysis

The analysis of a circuit output with respect to the time is called Transient analysis or timing analysis. The transient analysis of the PP-UVPCO is observed on Tanner Tool. The device is found to be linear as the output is fairly linear with respect to input with the passage of time as shown in Figure 5 below

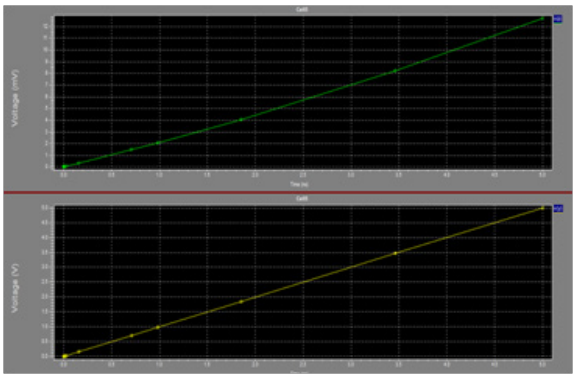

Figure 5 Transient analysis of device.

Mathematical regression analysis

The Regression statistics express the mathematical model of the device. It includes multiple R, R square and Adjusted R square, and Standard error value obtained during experiment. The various value obtained during the statistical analysis is shown in Table 1.

Table 1 Regression statistics

Regression	Statistics
Multiple R	0.998428255
R Square	0.99685898
Adjusted R Square	0.996662667
Standard Error	0.08121496
Observations	18

The linear trend line between the readings of V_y and V_z is plotted and the coefficient of determination R^2 is found to be 99.7% along with standard error of 0.081. The coefficient of determination and standard error are shown in Figure 6. R^2 (Coefficient of Determination) is useful because it gives the proportion of the fluctuation (variance) in other terms stability. This shows how one variable that is predictable from the other variable. That is why it is sometimes referred as predictive model. The coefficient of determination represents how well the regression line drawn from the data. If the regression line passes through each and every point on the scatter plot, this signifies that it would be easy to explain all the variations.

Residual plot

A residual plot is one of the statistical technique which is used to calculate how fit is regression model to your data. It should be random in nature the more the degree of randomness more the system is good to use. There should not be any recognizable pattern. The uncorrelated residuals models always give good value. Figure 7 shows random residual Plot for the device.

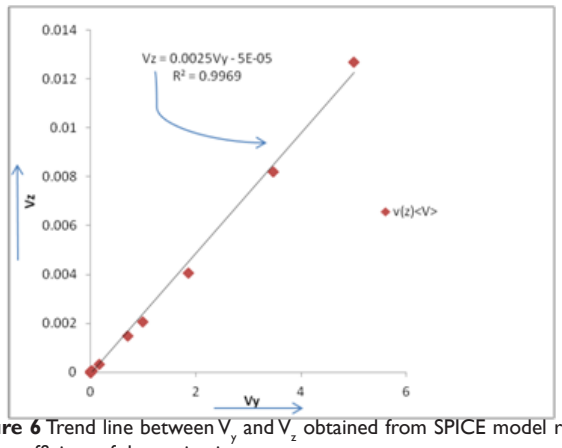

Figure 6 Trend line between V_y and V_z obtained from SPICE model readings with coefficient of determination.

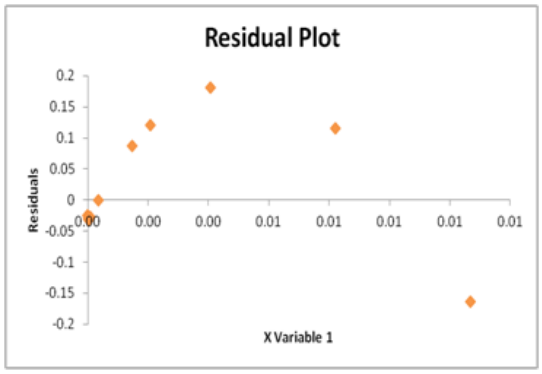

Figure 7 Residual plot for the device reading.

Normal probability plot

Normal Probability plot is the special case of probability plot which determines whether a given dataset can be uniformly distributed or not and also termed as a special case of the probability plot. If the points on this plot show a linear pattern, this indicates that the normal distribution is a good model for this data set. The figure 8 shows the normal distribution of the device dataset and it is clearly observed that the gradually linear increase in the values is a good model (Figure 8).

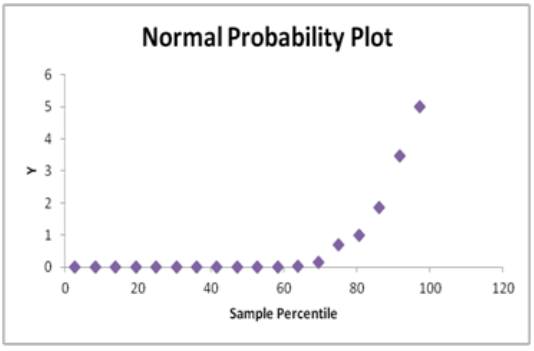

Figure 8 Normal probability plot.

Result analysis

The various results obtained are summarized in this section. On comparing new design with the existing design we arrive at following results

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1. Almost zero static power.
2. Only one capacitor is used in this technique.
3. Number of current sources deployed is zero in new device.
4. Number of n-MOS and p-MOS required: 8 and 1.
5. No resistor is required in the new technique.
6. Only one Voltage source required.

Table 2 Analysis of PP-UVPCO devices

Parameters	PP-UVPCO
Technology	Pseudo PMOS
Power supply(VDD, GND)	5V-0V
No.of Mosfets	9
Capacitor	1
Current Source	0
NMOS	8
PMOS	1
Resistor	0
Voltage Source	1
Max power (Watts)	3.000194e-002
Min power (Watts)	0.000000e+000
Stability analysis	Closed loop stable

Volumetric efficiency is the measures of performance of function per unit volume. In today's scenario of electronics, miniaturization and low power circuit is a need for almost all circuits. From this table analysis, we can figure out that there is significant saving in terms of Components as compared to CMOS technology. Hence, to meet our goal a new circuit which meets all our requirements in terms of component saving i.e miniaturization and power efficiency is simulated and proposed in this circuit.

Conclusion

In this research studies, a new device employing Pseudo PMOS-UVPCO is simulated. Pseudo PMOS Current Conveyor PPCC introduced as a basic building block in electronics circuits that provides a simplified approach to the design of linear analog systems. It consumes considerably low power and hence very useful for designing low power devices. The rate at which output changing with respect to the input i.e. slew rate also improved. A significant advantage of the proposed design is it's simple architecture and less number of component. Hence it is good for Air quality monitoring applications.

Future work

This study may be extended for further improvements in terms of power and size, besides the wiring and layout characteristics level.

Acknowledgments

None.

Conflicts of interest

The author declares there are no conflicts of interest.

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