

Review Article





# Simulation & performance analysis of various R2R D/A converter using various topologies

#### **Abstract**

This paper presents the study of R2R D/A converter using various topologies like CMOS, Transmission Gates (TG) and OP-AMP. For the sake of simplicity 4 bit input is taken. The R2R D/A converter consist of only two values of resistor R & 2R. By using the repetitive arrangement of precision resistor network in a ladder. The simulation of the R2R D/A converter has been done on the TANNER-EDA T-SPICE and the circuit verification has been done on S-EDIT on TANNER-EDA software package. Simulation results are included to demonstrate the results. The outcomes of simulation are fairly in agreement with the theoretical estimation.

**Keywords:** R2R D/A, CMOS, Op-amp, transmission gates

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#### Introduction

Most of the modern wireless communication systems require a wireless frequency (RF) subsystem.1 The design of RF system consists of various components ranging from connecting modules to power supply, antenna, baseband layer, and other interfaces, constitute a radio system.<sup>2-4</sup> The main front end radio transmitter module consists of digital signal processor which processes the input digital signal to analog output signal and visa versa. In other words, a discrete-amplitude; discrete-time digital input signal is converted into a continuous-amplitude, continuous-time analog counterpart. In most of the cases the input digital signal is a binary-coded representation of an analog signal using N bits. The leftmost bit of the input digital word is usually called the most-significant bit (MSB), and the rightmost bit is called the least-significant bit (LSB).5-7 Now with the advancements in VLSI technologies CMOS based current mode DACs are the very much for many applications. The main features of CMOS like their high speed, low power, and cost effectiveness enable it successful for the implementations in designing of circuits.<sup>8–10</sup> Nevertheless the digital to analog converter (DAC) can equally be used as a standalone chip for SoCs. There are several digital to analog architectures for DAC designs which includes resistor string, R2R ladder networks, charge scaling, current steering, and segmented current steering. 11-13 Common problem with DAC to avoid glitches because of the rapid change of more than one digital input bit at a sampling time causes noise problems since resistors are noise sources. Because of which DAC output dose not result in expected value.<sup>14-17</sup> In this research studies a comparative R2R DAC using various CMOS topologies has been presented. It is well known fact that the binary weighted resistor D/A converted requires a wide range of resistance value and matched switch for each bit position. 18-22 The R2R D/A converter with an R-2R ladder network which eliminates these complications at the expense of an additional resistor for each bit is shown in Figure 1. Bit MSB and LSB are driven from logic gates. The operation of this converter can be considering the weights of different bits one at a time. This can be followed by superposition to construct analog output corresponding to any digital input word.

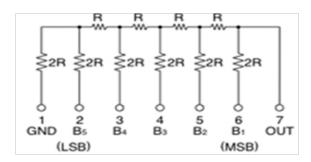


Figure I R2R D/A converter diagram.

## **R2R D/A converter using CMOS**

Figure 2 shows the R2R D2A converter using CMOS inverter. CMOS inverter is attached in series with next CMOS inverter for 1-bit and the R-2R series is attached with it, and then It gives output the same bit as input. The same process is repeated for all the bits. Figure 3 presents output in the analog form. The output Figure 3 of the R2 D/A converter is followed by the voltage as the voltage at node (n-1) is given by-  $V_{n-1} = V_R \left(\frac{R}{3R}\right) v$ 

$$V_{out} = -\frac{V_R}{2}$$
 The weight of MSB is  $-\frac{V_R}{2}$ 

## R2R D/A converter using TG

Transmission Gate (TG) is used in digital CMOS circuit design to pass or not pass a signal.  $^{23-25}$  In other words, it acts like switch. The gate is made up of the parallel connection of p- and n- channel MOSFET. When S is high then the transmission gate pass the signal on the input to the output. Transmission gate using CMOS and its circuit and symbols are shown in Figure 4–6. In the Figure 7 R2R D/A converter is using TG. In this  $b_0$ ,  $b_1$ ,  $b_2$  and  $b_3$  are the digital signal. The TG is a good switch and when the digital pulse is given to





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the entire bit it gives the output Figure 8 corresponding to the analog signal.

# R2R D/A converter using OP-AMP

The Figure 9 shows the internal circuit of op-amp which is used in the R-2R D/A converter using op-amp. When data is in binary form, the 0's and 1's where the logic zero may be a value up to 0.8 volts and the 1 may be a voltage from 3 to 5 volts. <sup>26–28</sup> The data can be converted to clean digital form using gates which are designed to be on or off depending on the value of the incoming signal. Data in clean binary digital form can be converted to an analog form by using a summing amplifier. For example, a simple 4-bit D/A converter can be made with an op-amp. Where the D's take the value 0 or 1. The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0. This is illustrated for 4 bits, but can

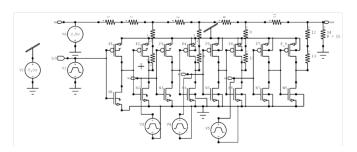


Figure 2 R2R D/A converter using CMOS.

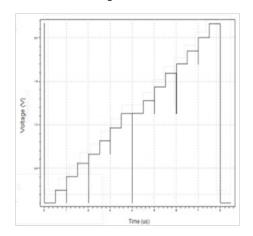


Figure 3 Output of D2A converter using CMOS.

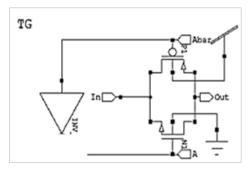


Figure 4 TG using CMOS.

be extended to any number with just the resistance values R and 2R. Input summing amplifier. More practical is the R-2R Network DAC. In the Figure 10, the negative input is at virtual ground, therefore the current through  $R_{TH} = 0$ .

Current through 2R connected to  $+5V = \frac{5V}{20} k\Omega = 0.25 mA$ 

The current will be the same as that in Rf.

$$V_{a} = -(20k\Omega)*(0.25mA) = -5V$$

Output voltage equation is given below.

$$V_{out} = R_f \left[ \frac{B_3}{2R} + \frac{B_2}{4R} + \frac{B_1}{8R} + \frac{B_0}{16R} \right]$$

The output is shown in Figure 11. with respective to the digital input and converting in analog output.

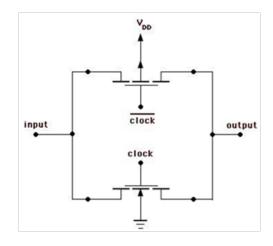


Figure 5 Circuit diagram of TG.

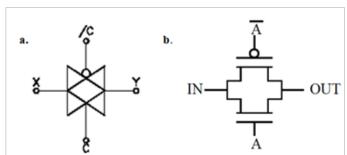


Figure 6 TG symbol a&b.

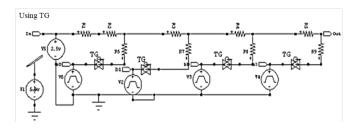


Figure 7 R2R D/A converter using TG.

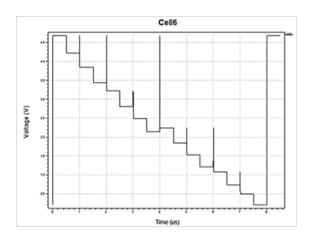


Figure 8 Output of D/A converter using TG.

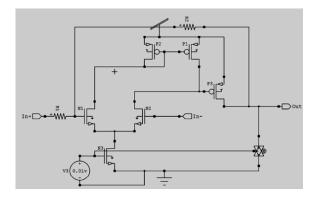


Figure 9 Internal structure of OP -AMP.

#### D/A using OP-AMP

Inference from Table 1: For the same technology i.e. CMOS technology developed for all the three design styles and the same power supply we arrive at the following comparative results:

Table I Comaprision analysis of various designs

Design style Properties	CMOS	ТG	OP-AMP
Technology used	CMOS	CMOS	CMOS
Power supply(VDD, GND)	3.5V-0V	3.5V-0V	3.5V-0V
Resistors	9	9	10
No. of components	16 MOS	4TG (8 MOS)	6 MOS
Average power dissipiation (Watts)	1.02E-02	3.80E-03	2.94E-02
Maximum power dissipiation (Watts)	9.67E-03	4.67E-03	4.13E-02

- a. Number of Components while implementing R2R D/A is least with OP-AMP as compared with other two design styles used.
- b. Power supply used in all the topologies remain fixed as shown in the table. 1.

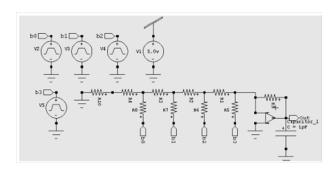


Figure 10 D/A converter using OP-AMP.

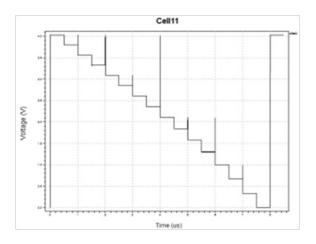


Figure 11 Output of D/A converter using OP-AMP.

- c. The number of resistors required in case of CMOS and TG is 9 while with OP-AMP it is one more. This indicates the area of fabrication with the earlier two is least.
- d. The average power dissipation for the above three cases in Watts is listed as:

CMOS -1.02e-002

TG - 3.80e-003

OP-AMP - 2.94e-002

From this we come down to the conclusion that the average power dissipated is maximum in case of OP-AMP based R2R D/A circuit and the minimum in the case of TG. The Maximum power dissipation for the above three cases in Watts is listed as:

CMOS -9.67e-003

TG - 4.67e-003

OP-AMP - 4.13e-002

From this we come down to the conclusion that the Maximum power dissipated is maximum in case of OP-AMP followed by CMOS and TG as indicated above.

#### Conclusion

In this paper, R2R D/A circuit employing various topologies like CMOS, TG, and OP-AMP is proposed. As a result of the various

analysis made we arrive at following important results

OP-AMP > CMOS > TG - The average and maximum power dissipation (in Watts)

CMOS > TG > OP-AMP- (Number of component used)

The above results shows that although the implementation of R2R D/A circuit with OP-AMP dissipated more power but it requires less number of components as compared with other two topologies. The various advantages of implementing R2R D/A circuit is that it's very easy principle of working and construction another one its fast conversion rate as compared to other circuits. These advantages responsible for its use in audio and video techniques.

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#### Conflict of interest

The author declares there is no conflict of interest.

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