MedCrave
Step into the World of Research

International Robotics & Automation Journal

Review Article

Open Access

CrossMark

Comparative study of various gates based in different technologies

Abstract

This paper provides the comparative study among various fabrication technologies for the same logical circuits based on NAND gate. The tool used for this analysis is Tanner which is an EDA tool and used for full custom designing of electronic circuits. The NAND gate is formed by CMOS only. The different technologies give varied output parameters with given input parameters. Hence, the main utilization of this study is to opt best suited technology for particular output parameter ranges for specified input parameter ranges for different applications based on logical gates. The conventional device generally used, consumes high power and is not stable with frequency variations. Therefore, a comparative analysis using different technologies is proposed, which has been useful for designing optimal conventional logics. The study is based on simulation of power consumption, noise analysis and frequency compensation technique of different gates.

Keywords: logical circuits, fabrication, tanner, CMOS

Volume 3 Issue 1 - 2017

Sanobar Chouhan,[1] Saurabh Chaudhary,[1] Tarun Upadhay,[1] Ajay Rupani,[1] Pawan Whig[2]

[1]Scholars, Jodhpur Institute of Engineering and Technology, India
[2]Vivekananda Institute of Professional Studies, India

Correspondence: Pawan Whig, Vivekananda Institute of Professional Studies, India, Email pawanwhig@gmail.com

Received: July 22, 2017 | **Published:** September 22, 2017

Introduction

The logic gates are electronic devices which produces logical output on basis of given one or more input.[1,2] Application of logic gates includes from small decision making devices, big calculating devices to huge super computers.[3,4] There are many logic gates to implement various Boolean logics among which two gates are considered universal. Charles Sanders Peirce showed in his work that designing of all basic logical gates is possible by using universal logical gates i.e. NAND & NOR.[5–7] But it was first published by Henry M Sheffer.[8] Here, we used NAND to study the change in output with different designing technologies. The used tool tanner is characterized by its five windows via S–edit, T–spice, W–edit, L–edit, and LVS. Using these one can analyse the circuit transients and can do AC and DC analyses. Now the questions arise are:

a. Why NAND only NOT NOR?

b. What are these different Technologies for designing?

c. Why these Technologies are defined by Length of Transistors?

The practical aspects of designing are sufficient for answering the above question and satisfactorily explain the consideration of NAND gate. These are explained as:

NAND only NOT NOR

a. Delay time in NAND gate is less than NOR gate: Series connection of PMOS increases the resistance of the circuit and hence delay time is more than NMOS.

b. Area required for NAND structure is less than NOR layout. The reason this is to get equivalent channel length for current modulation is more in NOR than NAND because the mobility of holes is approximately three times less than mobility of electrons.

c. There is less gate leakage current in NAND structure.

Size of transistors used for manufacturing is same for PMOS and NMOS in case of NAND gate whereas in NOR gate.

Different technologies and why are defined by length of transistor

The different technologies are predefined manufacturing parameters of electronics elements used for simulation and designing of circuits. In case of transistors they are defined by length of transistors.[9–11] Transistor length is used to define technologies instead of width of it because current modulation is characterized by channel length.[11–14]

Logic gates

NAND gate: This is a NOT–AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion (Figure 1).

NOT gate: The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way (Figure 2).

AND gate: The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB (Figure 3).

OR gate: The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation (Figure 4).

NOR gate: When OR gate is followed by NOT gate then NOR gate is formed. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion (Figure 5).

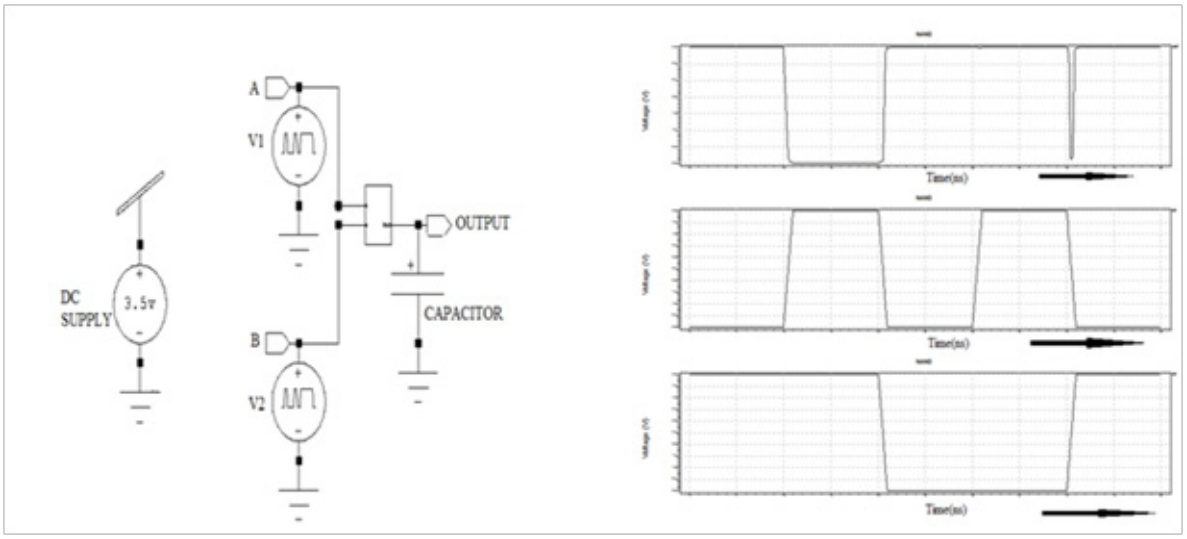

Figure 1 NAND gate circuit with its input- output waveforms.

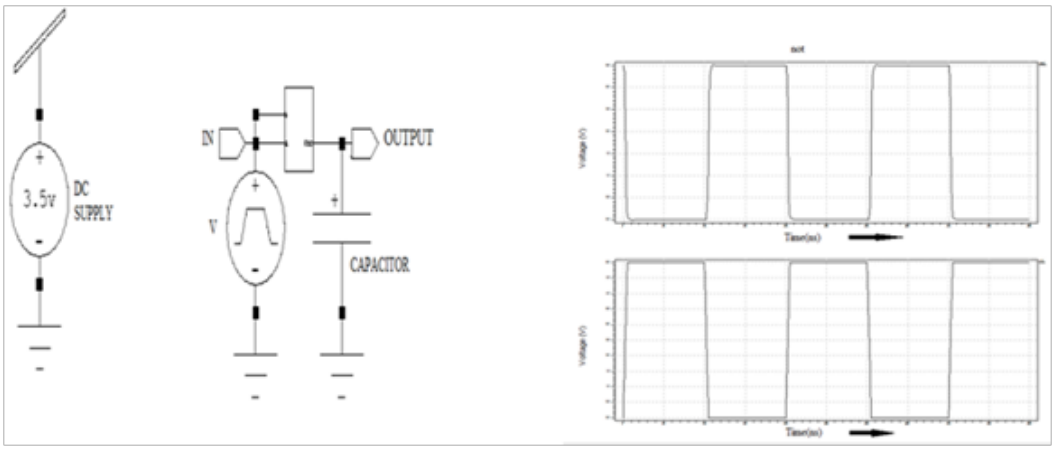

Figure 2 NOT gate circuit with its input- output waveforms.

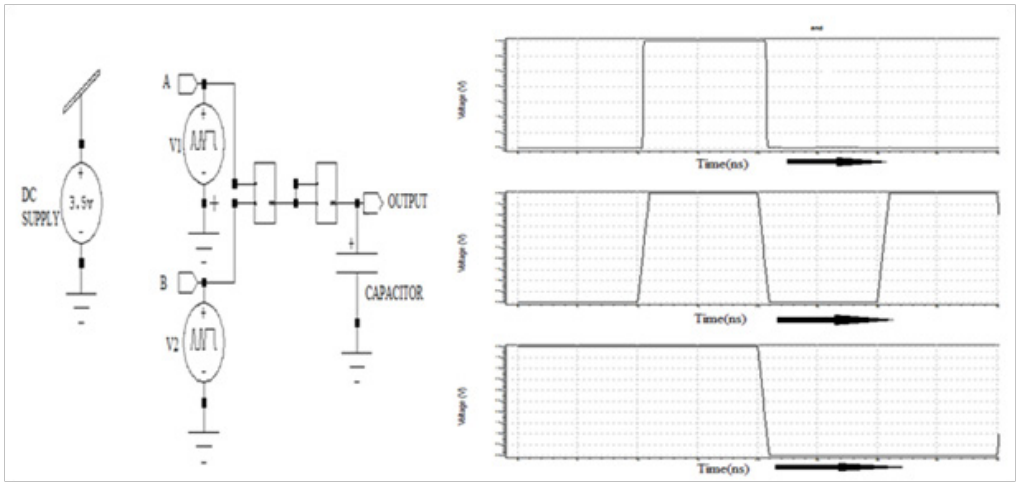

Figure 3 AND gate circuit with its input- output waveforms.

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046

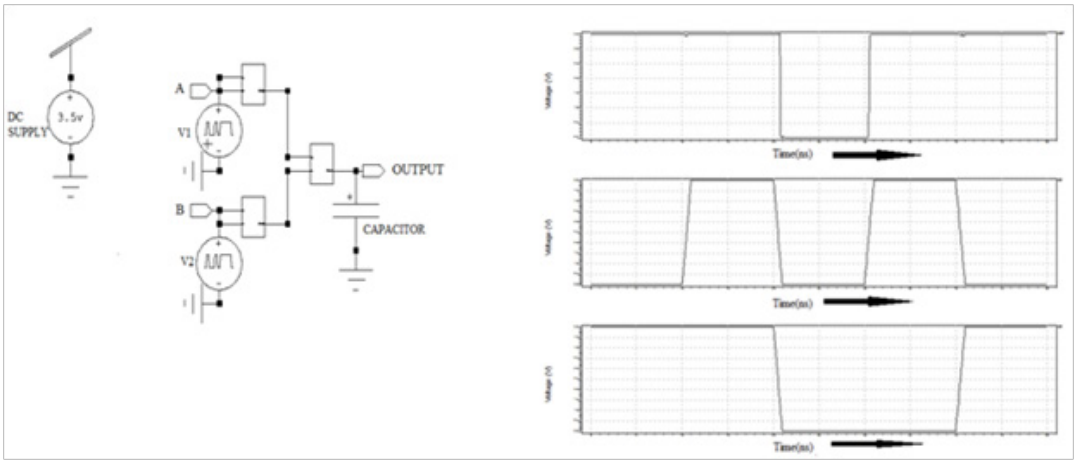

Figure 4 OR gate circuit with its input- output waveforms.

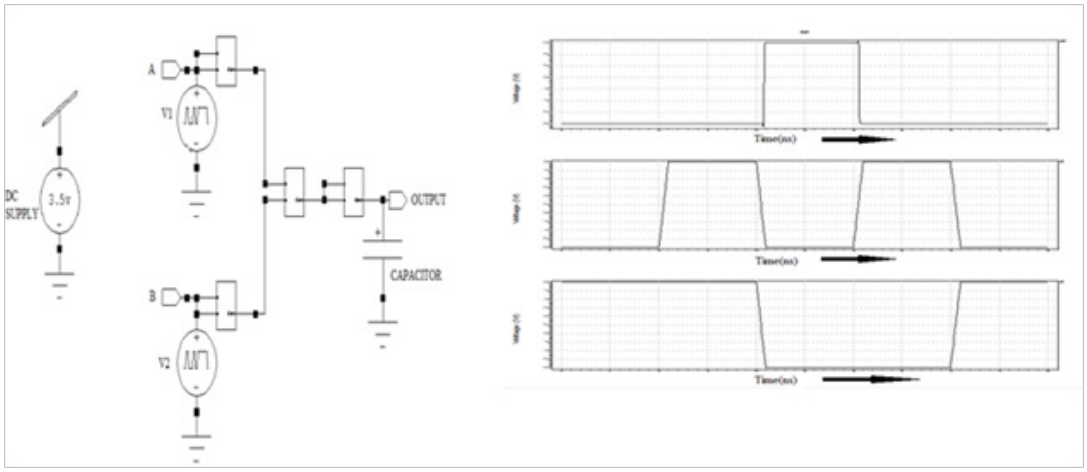

Figure 5 NOR gate circuit with its input- output waveforms.

Results after simulation of all circuits

Simulation of all above circuits designed in S–edit is done and various parameters like power consumption, input–output noise voltages and delay time etc. are obtained using T–spice and are summarized in the following Table (1–5).

Graphical representation of results

The results represented in form of pie–charts are as follows for better visualization (Figure 6–17).

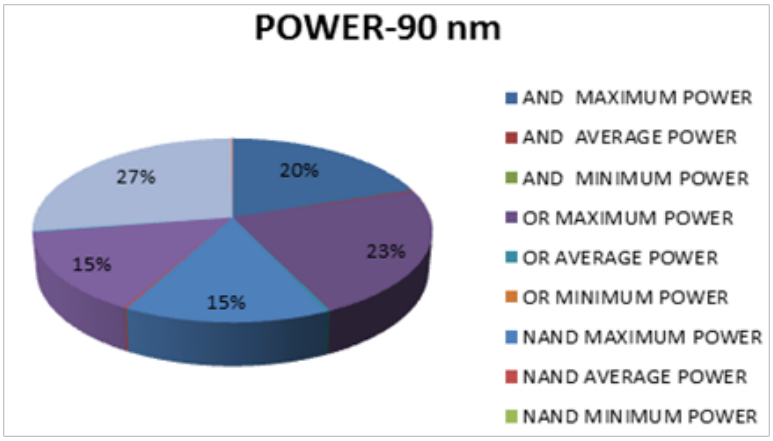

Figure 6 Pie Chart of Power Comparison of different gates using 90nm design file.

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046

Table 1 Power comparison

Power comparison of gates using different data files				
		Data files(in nm)		
GATES	Power(in watts)	90	180	250
	Maximum power	6.68E-03	1.11E-02	7.70.E-03
AND	Average power	1.22E-04	1.03E-04	1.01E-04
	Minimum power	7.06E-10	1.39E-04	1.32E-10
	Maximum power	9.17E-03	1.26E-02	8.84E-03
OR	Average power	1.51E-04	1.28E-04	1.21E-04
	Minimum power	1.12E-09	1.79E-10	1.60E-10
	Maximum power	4.93E-03	7.74E-03	5.63E-03
NAND	Average power	7.05E-05	7.30E-05	6.46E-05
	Minimum power	4.42E-12	1.41E-12	2.79E-11
	Maximum power	4.93E-03	7.74E-03	5.63E-03
NOT	Average power	7.05E-05	7.30E-05	6.46E-05
	Minimum power	4.42E-12	1.41E-12	2.79E-11
	Maximum power	1.08E-02	1.57E-02	1.05E-02
NOR	Average power	1.28E-04	1.17E-04	1.06E-04
	Minimum power	2.19E-10	2.12E-10	1.21E-10

Table 2 Noise voltage comparison

Noise voltage comparison				
		Data files(in nm)		
GATES	Measurement	90	180	250
AND	Input noise	24.38220uV	25.83463uV	27.02869uV
	Output noise	221.65349KV	12.28445XV	12.81874XV
OR	Input noise	24.38223uV	25.83465uV	27.02872uV
	Output noise	338.17777KV	16.55291XV	15.38984XV
NAND	Input noise	27.57381uV	21.13712uV	26.50244uV
	Output noise	820.03865mV	12.98139V	12.33618V
NOR	Input noise	27.57375uV	21.13710uV	26.50240uV
	Output noise	136.80313GV	174.22433TV	189.89311TV
NOT	Input noise	27.57381uV	21.13712uV	26.50244uV
	Output noise	321.79163mV	2.24458V	2.55462V

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046

Table 3 Rise time measurements table

Rise time measurements				
		Data files(in nm)		
GATES	Measurement	90	180	250
	Rise time	2.56E-09	1.34E-09	2.07E-09
AND	Trigger	2.09E-09	2.24E-09	2.25E-09
	Target	4.64.E-09	3.58.E-09	4.32E-09
	Rise time	2.57E-09	1.36E-09	2.08E-09
OR	Trigger	2.00E-09	2.19E-09	2.22E-09
	Target	4.56E-09	3.54E-09	4.30E-09
	Rise time	3.10E-09	2.36E-09	3.09E-09
NAND	Trigger	1.04E-07	1.03E-07	1.03E-07
	Target	1.07E-07	1.05E-07	1.06E-07
	Rise time	3.10E-09	2.36E-09	3.09E-09
NOT	Trigger	1.04E-07	1.03E-07	1.03E-07
	Target	1.07E-07	1.05E-07	1.06E-07
	Rise time	2.70E-09	1.39E-09	2.39E-09
NOR	Trigger	1.04E-07	1.03E-07	1.04E-07
	Target	1.07E-07	1.05E-07	1.06E-07

Table 4 Fall time measurements

Fall time measurements				
		Data files(in nm)		
GATES	Measurements	90	180	250
	Fall time	2.34E-09	2.83E-09	3.17E-09
AND	Trigger	1.03E-07	1.03E-07	1.03E-07
	Target	1.05E-07	1.05E-07	1.06E-07
	Fall time	2.45E-09	2.81E-09	3.16E-09
OR	Trigger	1.03E-07	1.03E-07	1.03E-07
	Target	1.05E-07	1.05E-07	1.06E-07
	Fall time	2.37E-09	2.61E-09	2.87E-09
NAND	Trigger	1.80E-09	2.02E-09	2.06E-09
	Target	4.16E-09	4.63E-09	4.93E-09
	Fall time	2.37E-09	2.61E-09	2.87E-09
NOT	Trigger	1.80E-09	2.02E-09	2.06E-09
	Target	4.16E-09	4.63E-09	4.93E-09
	Fall time	1.74E-09	2.08E-09	2.40E-09
NOR	Trigger	2.02E-09	2.31E-09	2.31E-09
	Target	3.76E-09	4.40E-09	4.71E-09

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046

Table 5 AC gain measurements

Ac gain measurements			
	Data files(in nm)		
GATES	90	180	250
AND	-9.43E+01	-9.93E+01	-9.81E+01
OR	-9.43E+01	-9.93E+01	-9.81E+01
NOT	-4.70.E+01	-5.25E+01	-5.08E+01
NOR	-1.41E+02	-1.51E+02	-1.48E+02
NAND	-4.70E+01	-5.25E+01	-5.08E+01

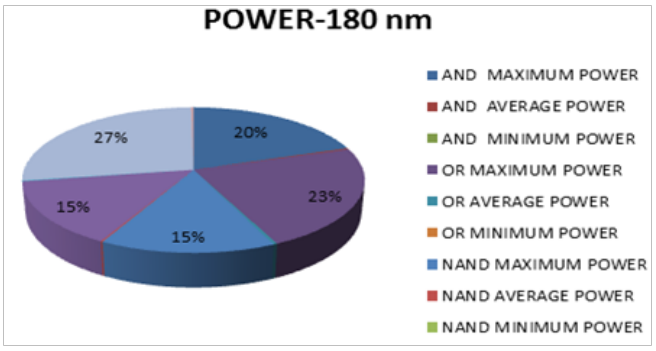

Figure 7 Pie Chart of Power Comparison of different gates using 180nm design file.

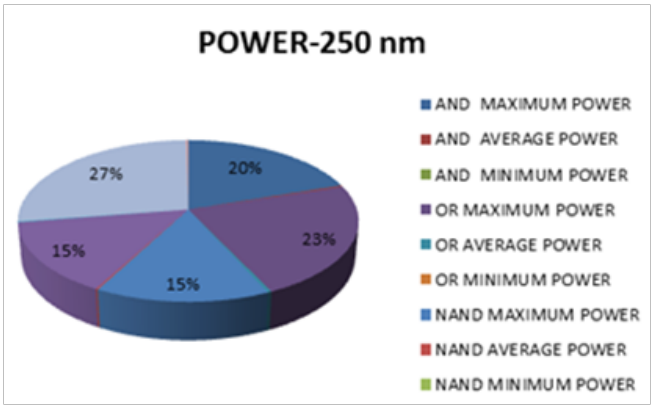

Figure 8 Pie Chart of Power Comparison of different gates using 250nm design file.

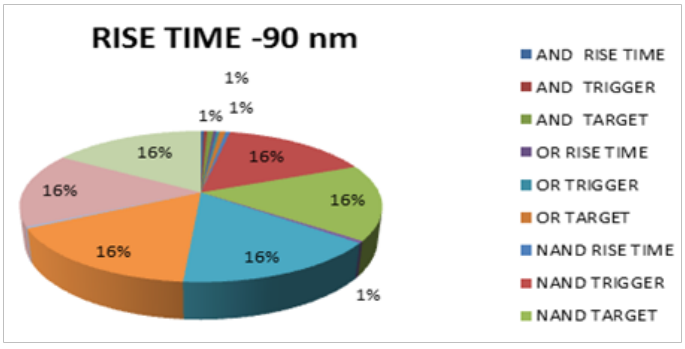

Figure 9 Rise Time Comparison of different gates using 90nm design file.

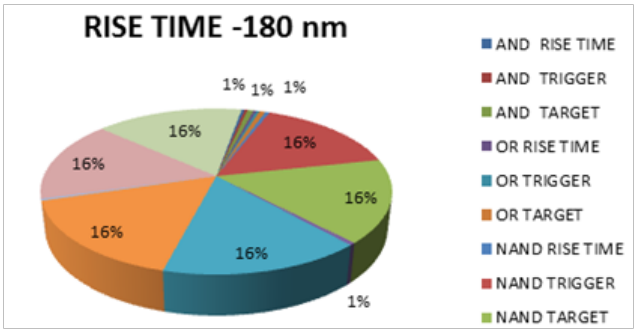

Figure 10 Rise Time Comparison of different gates using 180nm design file.

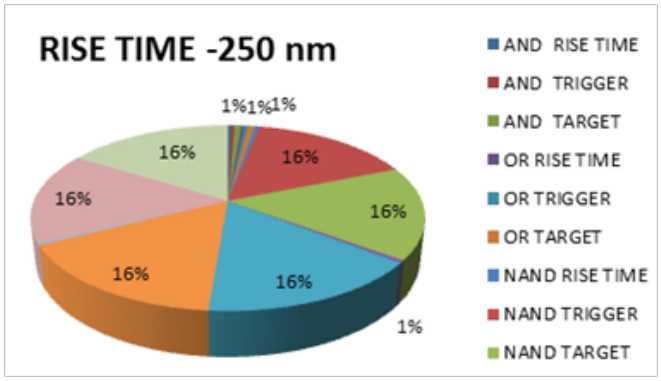

Figure 11 Rise Time Comparison of different gates using 250nm design file.

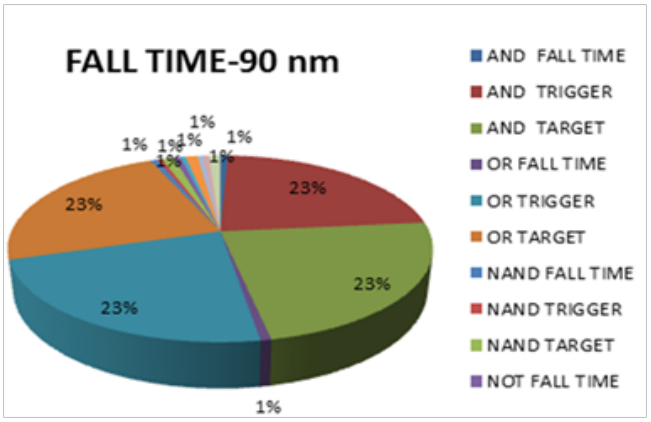

Figure 12 Fall Time Comparison of different gates using 90nm design file.

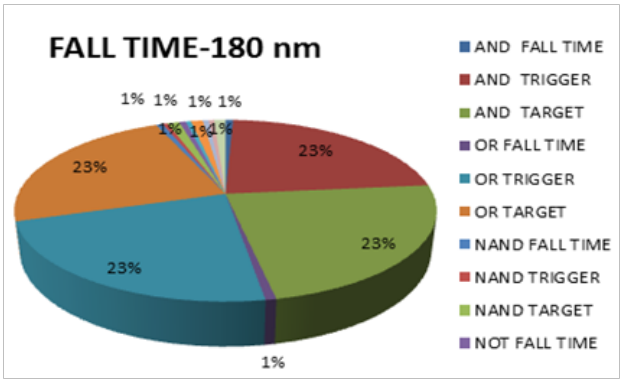

Figure 13 Fall Time Comparison of different gates using 180nm design file.

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046

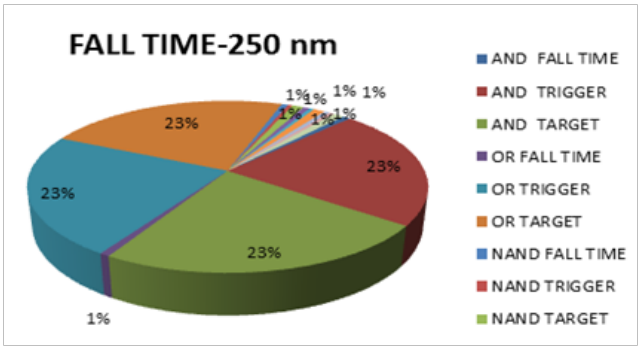

Figure 14 Fall Time Comparison of different gates using 250nm design file.

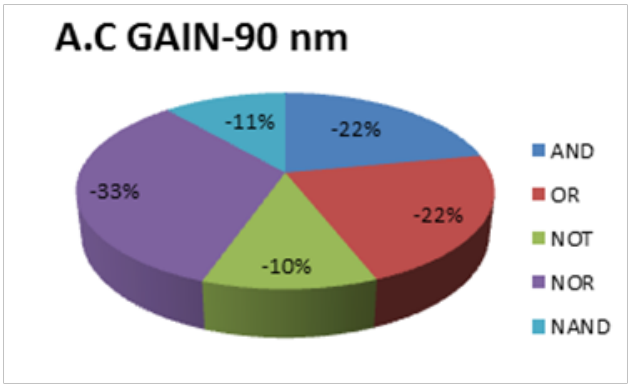

Figure 15 AC Gain Comparison of different gates using 90nm design file.

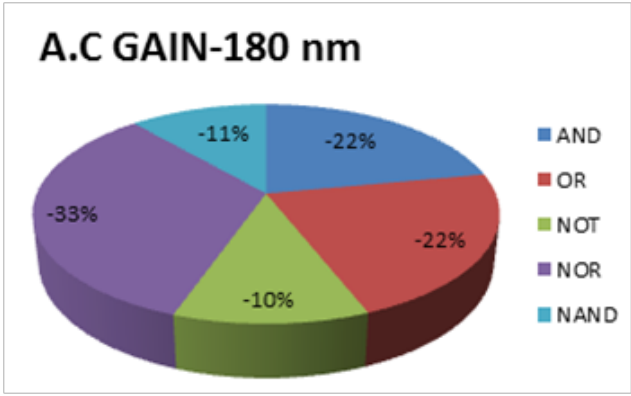

Figure 16 AC Gain Comparison of different gates using 180nm design file.

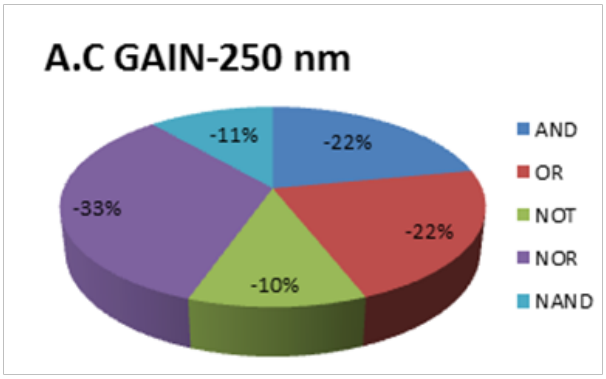

Figure 17 AC Gain Comparison of different gates using 250nm design file.

Conclusion

The result of above study can be concluded as following points:

a. It is known that decreasing the size of transistor the average power consumption increases with increment in minimum power and decrement in maximum power but the maximum power is highest and minimum power is minimum in 180nm.

b. The input noise in 180nm is minimum and output noise is decreasing with size thus if output noise can be improved by some means then 180nm technology will be the best technology among these three in terms of noise parameters.

c. 180nm has highest gain among three technology considered.

d. The fall time is decreasing with decrement in size with least rise time in 180nm technology thus total transit time of 180nm is minimum than other two.

Future work

This study may be extended for further improvements in terms of power and size, besides the wiring and layout characteristics level.

Acknowledgments

I would be highly grateful towards My Institute Vivekananda Institute of Professional studies and My wife Madhu and Son Anumaan Whig for their continuous support and a source of inspiration to complete my research studies. Moreover I would like to express my gratitude towards MedCrave Group for publishing my research article in their esteemed journal.

Conflict of interest

Author declares that there is none of the conflicts.

References

1. Bhoj Ajay N, JhaNiraj K. Design of Logic Gates and Flip–Flops in High–performance FinFET Technology. *IEEE transactions on very large scale integration (vlsi) systems*. 2013;21(11):1975–1988.
2. Wei L, Chen Z, Roy K. Double gate dynamic threshold voltage (DGDT) SOI MOSFETs for low power high performance designs. *Proc IEEE Int SOI Conf*. 1997. p. 82–83.
3. Rostami M, Mohanram K. Dual–Vth independent–gate FinFETs for low power logic circuits. *IEEE Trans Computer–Aided Design*. 2011;30(3):337–349.
4. Krambeck R, Lee C, Law H. High–speed compact circuits with CMOS. *IEEE J of Solid–State Circuits*. 1982;17(3):614–619.
5. Olivieri M. Design of synchronous and asynchronous variable–latency pipelined multipliers. *IEEE Trans on VLSI Systems*. 2001;9(2):365–376.
6. Balasubramanian, Bhuva BL, Black JD, et al. RHBD Techniques for Mitigating Effects of Single–Event Hits Using Guard–Gates. *IEEE transaction on nuclear science*. 2005;52(6):2531–2535.
7. Wirth I, Vieira MG, Kastensmidt FGL. Accurate and computer efficient modeling of single event transients in CMOS circuits. *IET circuits Devices Syst*. 2007;1(2):137–142.
8. Chen CL, Hsiao MY. Error correcting codes for semiconductor memory applications: A state–of–the–art review. *IBM J Res Develop*. 1984;28(2):124–134.
9. Weste NHE, Eshraghian K. *Principles of CMOS VLSI design*. 1988.p. 163–166.

10. Tausch HJ. Simplified birthday statistics and Hamming EDAC. *IEEE Transaction on nuclear science*. 2009;56(2):474–478.

11. Massobrio G, Antognetti P. *Semiconductor Device Modeling with SPICE*. 1993.

12. Whig P, Ahmad SN. A novel Pseudo NMOS integrated ISFET device for water quality monitoring. *Active and Passive Electronic Components*. 2013.

13. Whig P, Ahmad SN. Development of economical ASIC for PCS for water quality monitoring. *Journal of Circuits, Systems and Computers*. 2014;23(6):1–13.

14. Duffy JA. *Bonding, energy levels, and bands in inorganic solids*. 1990. p. 1–5.

Citation: Chouhan S, Chaudhary S, Upadhay T, et al. Comparative study of various gates based in different technologies. *Int Rob Auto J.* 2017;3(1):262–269. DOI: 10.15406/iratj.2017.03.00046