Review Article

Metal contacts to 2d-materials for device applications

Abstract

Atomically thin sheets of 2D-materials spanning over a reasonably large range of bad gap from zero in graphene to>6eV in hexagonal boron nitride (h-BN) with a number of unique optical, electronic, and thermal properties offer a whole range of engineered nano materials for designing and fabricating novel devices not yet known in conventional bulk semiconductors. Being a monolayer, these materials are not only very well suited for flexible electronics but also from different categories of hetero structures–laterally as well as vertically for having access to control charge carrier transport besides optical activities via excitonic formations. The most advantageous part of these 2D layered materials is their extra sensitivity to atomic, molecular and nano particulate material species when present there making them extremely sensitive to detect species in concentration not possible in conventional sensor materials. In order to exploit all these superlative features of these highly sensitive material species it is equally challenging to apply the conventional device fabrication techniques for their device properties. The experimental work done in this context are examined here in this review to assess the current status and future prospects of these emerging novel material still awaiting for their applications in fields like printed micro/nano sensors, large area electronics and intelligence in upcoming fields of Internet of Things and other areas of robotics for instance in future.

Keywords: 2D-semiconductors, metal-semiconductor contacts, planar contacts, edge contacts, 2D-FET Structures, schottky barrier heights, fermi level pinning

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Introduction

With the discovery of a new semiconducting material, it is first of all necessary to characterize it in terms of its temperature dependent conductivity, mobility, and carrier concentration besides optical transitions to establish about its possible uses in fabricating electronic and optoelectronic devices with specific functions. Next comes the design of device structure to realize the targeted device behavior by involving a number of layers according to the requirements. Out of all these exercises, the choice of contact to have access to the input and output regions of the device is very critical. In case the contact resistance of the interface involved in metal-semiconductor contact is not appropriate, the device functions will be lost.[1] When a metal is deposited on a semiconductor, in general it establishes a Schottky contact creating a potential barrier depending upon the work function of the metal and the electron/hole affinity of the semiconductor. Higher Schottky barrier leads to rectifying contact but in case it is close to zero it forms an ohmic contact. This whole concept of metal-semiconductor contacts in conventional semiconductors have already been studied and developed commercially for fabricating devices and circuits in form of ICs.[1] In case of 2D-semiconductors besides the absence of dangling bonds on the surfaces on either side the anisotropic conduction gives rise to very high contact resistance due to large Schottky barrier height or even Fermi level pinning. Keeping this anisotropy in view, even edge contacts have been explored similar to those used in HEMT devices for which the technology has been established up to commercial level.[1,2] The theoretical studies have found the sensitivity of the electronic structure of 2D-semiconductor responsible for high contact resistance. Still theoretical studies are going on to study the influence of some external species in making the interface more controlled. For example, applying quantum theoretical considerations, the minimum contact resistance is expected to be two orders magnitude less than practically observed. This shows that there is still scope for improving the behavior of these 2D-semiconductor based devices considerably.[2]

An attempt has been made to assess the current status and future prospects of forming high quality contacts for their device applications in near future. Fabrication of low contact resistance in 2D mono/multiple layer devices is essential for high I_{on} current, large photo response and high-frequency operation.[3,4] The large contact resistance observed at the 2D mono/multiple layer-3D metal interface, however, constrains the drain current.[5–7] Contacting 2D mono/multiple layer poses a number of experimental and conceptual problems. Theoretically, properties of the interface are governed by the chemical interaction between the metal and the mono/multiple layer. Substitution doping, a common method of reducing the contact resistance in bulk semiconductors, is not possible to extend here as it would modify both the 2D material and its properties. Further, the surface with no dangling bonds of a 2D mono/multiple layer makes it difficult to form interface bonds with a metal, thereby increasing contact resistance. The quantum limit to the contact resistance determined by considering the number of conducting modes within the channel,[8,9] which is connected to the 2D charge carrier density, gives $R_{Cmin} \sim 30$ Ω. μm at $n_{2D} = 10^{13}$ /cm^2, which is three orders of magnitude lower than the typical contact resistance to monolayer MoS_2.[10] This shows that there is plenty of room for improving the interface properties by studying the physics of contacts between metals and 2D mono/multiple layer. [2]

Planar contacts

For fabricating good ohmic contact between a metal and 2D-semiconductor it is necessary to understand the charge carrier transport across a 2D-semiconducting mono/multiple layers and metal interface. In this context, it is helpful to recapitulate the conventional model of metal-semiconductor junction studied since long.[1] In a

conventional metal-semiconductor junction, the Schottky barrier (SB) height decides whether it would be ohmic, or Schottky contact (i.e. rectifying) in nature. The SB height is defined as the difference between metal work function and affinities of electrons and holes measured from the conduction and valence band edges, respectively, in n and p-type semiconductors. The alignment of the semiconductor's bands near the junction being ideally independent of the semiconductor's doping level, the *n*-type and *p*-type SB heights ideally add to the band gap E_G. In case of significantly large SB height (i.e. $\gg k_B T$), the semiconductor next to the interface is depleted offering a potential barrier. The transport of charge carriers across such a potential barrier has been modeled by thermionic emission involving carriers within the thermal energy $k_B T$ around the energy equal to the barrier height.[11] For significantly lower SB heights, the semiconductor remains almost un depleted and offers ohmic contact behavior due to carrier tunneling. Under normal doping conditions, it is a mix of thermionic emission and tunneling together that represents the current–voltage characteristics.[12] Ideally, it is possible to reduce SB height by doping the semiconductor to either n^{++} or p^{++} level (i.e. heavy doping) favoring mostly charge carrier tunneling across the SB.

However, under practical conditions, there are invariably significant deviations from these ideal conditions, which ultimately give rise to interface states having their energies in the band gap. Depending upon the distribution of these interface states across the band gap the alignment of Fermi level gets clamped if sufficient density of states are there and form double layer in the semiconductor next to the filled surface states from the electrons supplied by the metal that screen the rest of the semiconductor from the influence of the work function of the metal. In such cases, the SB height becomes independent of the metal work function and this phenomenon is known as FL pinning.[13] In general, the presence of interface states having energy levels inside the band gap makes the whole situation quite complex. The role of these deviations will be referred back and forth while examining the cases of 2D-semiconductors as will be seen while discussing the specific cases. The efficient integration of 2D functional layers with three-dimensional (3D) systems being a challenge and limiting device performance, and circuit design, the experimental investigations made in this context were reviewed recently by analyzing the heterojunctions formed between 2D-3D materials. The contact resistivity of metal on graphene and related 2D materials deserves special attention, while the Schottky junctions formed between metal/2D semiconductor and graphene/3D semiconductor call for careful reconsideration of the physical models describing the junction behavior. The combination of 2D and 3D semiconductors forming a *p–n* junction are currently being realized and characterized.[14] Device designs of 2D-FETs were presented on the basis of understanding of source/drain contacts for harvesting the intrinsic properties of MoS_2 finding a right choice of number of MoS_2 layers. Using scandium contacts on 10-nm-thick exfoliated MoS_2 flakes that are covered by a 15 nm Al_2O_3 film, effective mobility~700 cm²/Vs was achieved at room temperature. The confusion arising out of linear current-drain voltage characteristics was also clarified.[15]

CNT and MoS_2 field-effect transistors were reported with asymmetric source-drain contact, from which the current directionality was found and different contact resistances were estimated under the two current directions. By designing various structures, it was concluded that the asymmetric electrical performance was caused by the difference in the effective Schottky barrier height (Φ_{SB}) caused by the different contacts. A detailed temperature-dependent study

was used to extract and compare the Φ_{SB} for both contact forms of CNT and MoS_2 devices; it was noted that the Φ_{SB} for the metal-on-semiconductor form was much lower than that of the semiconductor-on-metal form and is suitable for all p-type, n-type, or am bipolar semiconductors. This observation was meaningful with respect to the design and application of nano material electronic devices. Additionally, using the difference in barrier height caused by the contact forms, Schottky barrier diodes were fabricated with a current ratio up to 10^4; rectifying circuits consisting of these diodes were able to work in a wide frequency range. This design avoided the use of complex chemical doping or hetero junction methods to achieve fundamental diodes that are relatively simple and use only a single material; these may be suitable for future application in nano electronic radio frequency or integrated circuits.[16] MoS_2 has been intensively investigated out of many 2D layered materials because of its unique properties in various electronic and optoelectronic applications with different band gap energies from 1.29 to 1.9 eV with the number of layers decreasing. To control the MoS_2 layers, atomic layer etching (ALE) was used. It consisted of cyclic etching of a radical-adsorption step such as Cl adsorption and a reacted-compound-desorption step via a low-energy Ar^+-ion exposure. This turned out to be a highly effective technique to avoid inducing damage and contamination that occur during the reactive steps. Whereas graphene is composed of one-atom-thick layers, MoS_2 is composed of three-atom-thick $S_{(top)}$-$Mo_{(mid)}$-$S_{(bottom)}$ layers; therefore, the ALE mechanisms of the two structures are significantly different. In this study, for MoS_2 ALE, the Cl radical is used as the adsorption species and a low-energy Ar^+ ion is used as the desorption species. A MoS_2 ALE mechanism (by which the $S_{(top)}$, $Mo_{(mid)}$, and $S_{(bottom)}$ atoms are sequentially removed from the MoS_2 crystal structure due to the trapped Cl atoms between the $S_{(top)}$ layer and the $Mo_{(mid)}$ layer) is reported according to the results of an experiment and a simulation. In addition, the ALE technique showed that a monolayer MoS_2 field effect transistor (FET) fabricated after one cycle of ALE is undamaged and exhibits electrical characteristics similar to those of a pristine monolayer MoS_2 FET. This technique is also applicable to all layered TMD materials, such as tungsten disulfide (WS_2), molybdenum diselenide ($MoSe_2$), and tungsten diselenide (WSe_2).[17]

A simple method of fabricating TMD hetero structures was reported containing $MoSe_2$ QDs and a MoS_2 or WSe_2 monolayer. The strong modification of photoluminescence and Raman spectra that includes the quenching of $MoSe_2$ QDs and the varied spectral weights of trions for the MoS_2 and WSe_2 monolayers were observed, suggesting the charge transfer occurring in these TMD hetero structures. Such optically active hetero structures conveniently fabricated by dispersing TMD QDs onto TMD monolayers are likely to have various nano photonic applications because of their versatile and controllable properties.[18] The transport properties of a prototype multilayer MoS_2/ WSe_2 hetero junction were reported *via forming* a tunable charge inversion/depletion layer. This layer was prepared at the surface of WSe_2 due to its relatively low doping concentration compared to that of MoS_2, which can be tuned by the back-gate bias. The depletion region was limited within a few nanometers in the MoS_2 side, while charges are fully depleted on the whole WSe_2 side, which were confirmed by Raman spectroscopy and transport measurements. Charge transport through the hetero junction was influenced by the presence of the inversion layer involving two regimes of tunneling and recombination. Furthermore, photocurrent measurements clearly revealed recombination and space-charge-limited behaviors, similar

to those of the hetero structures built from organic semiconductors.[19] The band engineering of semiconductor hetero junctions for atomically thin optoelectronic devices was studied by preparing van der Waals hetero structures. With type II band alignment, interlayer excitons, where Coulomb bound electrons and holes are confined to opposite layers, have shown promising properties for novel excitonic devices, including a large binding energy, micron-scale in-plane drift-diffusion, and a long population and valley polarization lifetime. Demonstrate the interlayer exciton optoelectronics based on electro statically defined lateral p–n junctions was demonstrated in a $MoSe_2$–WSe_2 hetero bi-layer. Applying a forward bias generated electroluminescence from interlayer excitons. At zero bias, the p–n junction functioned as a highly sensitive photo detector, where the wavelength-dependent photocurrent measurement allowed the direct observation of resonant optical excitation of the interlayer exciton. The resulting photocurrent amplitude from the interlayer exciton was about 200 times smaller than the resonant excitation of intra layer exciton. This implied that the interlayer exciton oscillator strength was 2 orders of magnitude smaller than that of the intra layer exciton due to the spatial separation of electron and hole to the opposite layers. These results formed the foundation for exploiting the interlayer exciton in future 2D hetero structure optoelectronic devices. [20]

A novel technological method was reported to fabricate sub-10 nm gaps with sharp edges and steep sidewalls. The realization of sub-10 nm gaps was derived from a corrosion crack along the cleavage plane of Bi_2O_3. By this method, ultrathin body field-effect transistors (FETs), consisting of 8.2 nm channel length, 6 nm high-k dielectric, and 0.7 nm monolayer MoS_2, exhibited no short channel effects. The corresponding current on/off ratio and sub threshold swing reaches to 10^6 and 140mV/decade, respectively. Moreover, integrated circuits with sub-10 nm channel operated as digital inverters with high voltage gain. These results suggested that using this method could be used to fabricate the ultra short channel nano patterns for the experimental groundwork for 2DMs FETs with sub-10 nm channel length and 2DMs integrated circuits.[21] Electrical metal contacts to two-dimensional (2D) semiconducting transition metal dichalcogenides (TMDCs) are found to be the key bottleneck in realizing the device performance due to strong Fermi level pinning and high contact resistances (R_c). Until now, Fermi level pinning of monolayer TMDCs has been reported only theoretically, although that of bulk TMDCs has been reported experimentally. Here, we report the experimental study on Fermi level pinning of monolayer MoS_2 and $MoTe_2$ by interpreting the thermionic emission results. In a recent work the experimental measurements were compared with the theoretical simulation results of the monolayer structure as well as the experimental results of the bulk structure. The pinning factor was estimated to be 0.11 and −0.07 for monolayer MoS_2 and $MoTe_2$, respectively, suggesting a much stronger Fermi level pinning effect, a Schottky barrier height (SBH) lower than that by theoretical prediction, and interestingly similar pinning energy levels between monolayer and bulk MoS_2. These results further imply that metal work functions have very little influence on contact properties of 2D-material-based devices. Moreover, it was noted that R_c was exponentially proportional to SBH, and these processing parameters could be controlled sensitively upon chemical doping into the 2D materials.[22]

In search of an improved strategy for low-resistance contacts to semiconducting transition metal di chalcogenides, *ab initio* DFT electronic structure calculations were carried out for $NbSe_2$/WSe_2 interface with quantum transport measurements of the corresponding hetero junction between a few-layer WSe_2 semi conductor and a metallic $NbSe_2$ layer. The theoretical results suggested that, besides a rigid band shift associated with charge transfer; the presence of $NbSe_2$ does not modify the electronic structure of WSe_2. Since the two transition metal dichalcogenides are structurally similar and display only a small lattice mismatch, their hetero junction could efficiently transfer charge across the interface. These findings were supported by transport measurements for WSe_2 field-effect transistors with $NbSe_2$ contacts, which exhibited nearly ohmic behavior and phonon-limited mobility in the hole channel, indicating that the contacts to WSe_2 were highly transparent.[23] In one of the experiments, graphene–WS_2 hetero junctions were prepared over large areas using a seedless ambient-pressure CVD technique. Techniques like Kelvin probe force microscopy, photo luminescence spectroscopy, and scanning tunneling microscopy were used to characterize the doping in graphene–WS_2 hetero junctions as-grown on sapphire and transferred to SiO_2 with and without thermal annealing. Both p–n and n–n junctions were observed, and a flat-band condition (zero Schottky barrier height) was found for lightly n-doped WS_2, promising low-resistance ohmic contacts. This indicated a more favorable band alignment for graphene–WS_2 than has been predicted, likely explaining the low barriers observed in transport experiments on similar hetero junctions. Simulations demonstrated that the large depletion width of the graphene–WS_2 junction reflected the electrostatics of the one-dimensional junction between two-dimensional materials.[24] Stacked van der Waals (vdW) hetero structures were contacted by overlaid graphene electrodes enabling atomically thin, flexible electronics. Using the first-principles quantum transport simulations of graphene-contacted MoS_2 devices to show how the transistor effect critically depends on the stacking configuration relative to the gate electrode. This could be traced to the stacking-dependent response of the contact region to the capacitive electric field induced by the gate. The contact resistance is a central parameter and the observation established an important design rule for ultrathin devices based on 2D atomic crystals.[25] In one of the studies carefully designed aqueous droplet light heating system was used along with a thorough mathematical procedure, which combined leads to a precise determination of internal light-to-heat conversion efficiency of a variety of nano materials. The internal light-to-heat conversion efficiency of Ti_3C_2, was measured to be 100%, indicating a perfect energy conversion. Furthermore, a self-floating MXene thin membrane was prepared by simple vacuum filtration and the membrane, in the presence of a rationally chosen heat barrier, produced a light-to-water-evaporation efficiency of 84% under one sun irradiation, which is among the state of art energy efficiency for similar photo thermal evaporation system. The outstanding internal light-to-heat conversion efficiency and great light-to-water evaporation efficiency reported in this work suggest that MXene is a very promising light-to-heat conversion material deserving further explorations.[26]

A novel MAX ceramic biomaterial was reported for the first time exhibiting the unique functionality for the photo thermal ablation of cancer upon being exfoliated into ultrathin nano sheets within atomic thickness (MXene). Biocompatible Ti_3C_2 nano sheets were synthesized based on a two-step exfoliation strategy of Ti_3AlC_2 by the combined HF etching and TPAOH intercalation. Especially, the high photo thermal-conversion efficiency and *in-vitro*/*in-vivo* photo thermal ablation of tumor of Ti_3C_2 nano sheets (MXenes) were revealed and demonstrated, not only in the intravenous administration of soybean phosphor lipid modified Ti_3C_2 nano sheets but also in the

localized intra-tumoral implantation of a phase-changeable PLGA/ Ti_3C_2 organic–inorganic hybrid. This study offered sufficient potentials of Ti_3C_2 nano sheets as a novel ceramic photo thermal agent used for cancer therapy.[27] A study reported about the contacts formed onto the surface of various metals and single-layer $MoSe_2$. Partial Fermi level pinning was demonstrated by the first-principle calculations, which indicated modulation of the electron Schottky barrier. Upon inserting a VS_2 layer between $MoSe_2$ layer and metal electrodes, all the n-type contacts at $MoSe_2$/metal interfaces turned into p-type, and the hole Schottky barrier could be tuned effectively by varying metal electrodes. The high work function of the VS_2 layer exerted significant influence on the band realignment of $MoSe_2$, making all the n-type contacts at $MoSe_2$/metal interfaces become p-type contacts at $MoSe_2$/ VS_2–metal interfaces. Variation of the Schottky barriers and band alignments with the work function of metal electrodes demonstrated a partial Fermi level pinning at the interfaces of $MoSe_2$/metal and $MoSe_2$/VS_2–metal. The partial Fermi level pinning resulted from the low density of interfacial states, which could be reflected partly by the interaction between $MoSe_2$ layer and metal electrodes.[28]

Monolayer MoS_2 is a direct band gap semiconductor with a band gap of 1.8eV. Recently, field-effect transistors were demonstrated using a mechanically exfoliated MoS_2 monolayer, showing promising potential for next generation electronics. The ultimate performance limit of MoS_2 transistors was estimated by using non equilibrium Green's function based quantum transport simulations showing that the strength of MoS_2 transistors lies in large ON–OFF current ratio ($>10^{10}$), immunity to short channel effects (drain-induced barrier lowering 10mV/V), and abrupt switching (sub-threshold swing as low as 60mV/decade). Our comparison of monolayer MoS_2 transistors to the state-of-the-art III–V materials based transistors, reveals that while MoS_2 transistors may not be ideal for high-performance applications due to heavier electron effective mass ($m^* = 0.45m_o$) and a lower mobility, they can be an attractive alternative for low power applications thanks to the large band gap and the excellent electrostatic integrity inherent in a two-dimensional system.[29] Discrete electronic and optoelectronic components like FETs, sensors, and photo detectors made from few-layer MoS_2 showed promising performance as a substitute of Si in conventional electronics and of organic and amorphous Si semiconductors in ubiquitous systems and display applications. The next step is to fabricate fully integrated multistage circuits and logic building blocks on MoS_2 to demonstrate its capability for complex digital logic and high-frequency ac applications. This was demonstrated in an inverter, a NAND gate, a static random access memory, and a five-stage ring oscillator based on a direct-coupled transistor logic technology. The circuits consisted of 2 to 12 transistors seamlessly integrated side-by-side on a single sheet of bilayer MoS_2. Both enhancement-mode and depletion-mode transistors were fabricated thanks to the use of gate metals with different work functions.[30] The electronic properties of graphene in contact with monolayer and bilayer $PtSe_2$ were studied using first-principles calculations. It turned out that there is no charge transfer between the components because of the weak van der Waals interaction while calculating the work functions of monolayer and bilayer $PtSe_2$ and analyzing the band bending at the contact with graphene. The formation of an n-type Schottky contact with monolayer $PtSe_2$ and a p-type Schottky contact with bi layer $PtSe_2$ was demonstrated. The Schottky barrier height was very low in the bilayer case and could be reduced to zero by 0.8% biaxial tensile strain.[31]

Atomically thin 2D materials are difficult to fabricate without degradation of the original properties of the material required in realizing 2D-material devices. Atomic layer deposition (ALD) was found an ideal technique for adding materials with atomic scaling precision to nano materials. Due to the surface-sensitive reactions of ALD, growth on 2D materials is strongly affected by the surface properties of the 2D materials. In this Perspective, ALD growth on 2D materials is reviewed and discussed with previously reported results to provide insights for investigating 2D materials.[32] Atomically thin MoS_2 is an ideal semiconductor material for FETs with sub-10 nm channel lengths. The high effective mass and large band gap of MoS_2 minimize direct source–drain tunneling, while its atomically thin body maximizes the gate modulation efficiency in ultra short-channel transistors. However, no experimental study to date has approached the sub-10 nm scale due to the multiple challenges related to nanofabrication at this length scale and the high contact resistance traditionally observed in MoS_2 transistors. Using semiconducting-to-metallic phase transition of MoS_2, a recent study demonstrated sub-10 nm channel-length transistor fabricated by directed self-assembly patterning of mono and tri layer MoS_2. This was done in a 7.5 nm half-pitch periodic chain of transistors where semiconducting (2H) MoS_2 channel regions were seamlessly connected to metallic-phase (1T′) MoS_2 access and contact regions. The resulting 7.5 nm channel-length MoS_2 FET gave low off-current of 10 pA/µm, an on/off current ratio of $>10^7$, and a sub threshold swing of 120 mV/ decade. The experimental results presented in this work, combined with device transport modeling, reveal the remarkable potential of 2D MoS_2 for future sub-10 nm technology nodes.[33] A novel approach was reported from a recent work for achieving low-resistance contacts to MoS_2 transistors with the intrinsic performance of the MoS_2 channel preserved. Through a dry transfer technique and a metal-catalyzed graphene treatment process, nickel-etched-graphene electrodes were fabricated on MoS_2 that yielded contact resistance as low as 200Ω·µm. The substantial contact enhancement (~2 orders of magnitude), as compared to pure nickel electrodes, was attributed to the much smaller work function of nickel-graphene electrodes, together with the fact that presence of zigzag edges in the treated graphene surface enhanced the tunneling between nickel and graphene. To this end, the successful fabrication of a clean graphene–MoS_2 interface and a low resistance nickel–graphene interface was critical for the experimentally measured low contact resistance.[34] A new strategy was demonstrated by fabricating 2D/2D low-resistance ohmic contacts for a variety of transition metal dichalcogenides (TMDs) using van der Waals assembly of substitutionally doped TMDs as drain/ source contacts and TMDs with no intentional doping as channel materials. It could be demonstrated that few-layer WSe_2 FETs with 2D/2D contacts exhibited low contact resistances of~0.3kΩ.µm, high on/off ratios $>10^9$, and high drive currents exceeding 320µA/ µm. These characteristics were combined with a two-terminal field-effect hole mobility μ_{FE} ~200cm^2/Vs at room temperature, which increases to>2000cm^2/Vs at cryogenic temperatures. A similar performance was observed in MoS_2 and $MoSe_2$ FETs with 2D/2D drain and source contacts. The 2D/2D low-resistance ohmic contacts presented here represented a new device paradigm that could take care of a significant bottleneck in the performance of TMDs and a wide variety of other 2D materials as the channel materials in post silicon electronics.[35] The origin of the improved contact properties of alloyed 2D metal–semiconductor heterojunctions were studied in a recent work by fabricating WSe_2 transistors with mixed transition layers containing van der Waals (M–vdW, $NbSe_2$/$W_xNb_{1-x}Se_2$/WSe_2)

junctions realizing atomically sharp interfaces, exhibiting long hot-carrier lifetimes of approximately~75,296s (78 times longer than that of metal–semiconductor, Pd/WSe$_2$ junctions). Such dramatic lifetime enhancement in M–vdW-junction devices was attributed to the synergistic effects arising from the significant reduction in the number of defects and the Schottky barrier lowering at the interface. Formation of a controllable mixed-composition alloyed layer on the 2D active channel could be a breakthrough approach to maximize the electrical reliability of 2D nano material-based electronic applications.[36] A recent research study of n- and p-type carrier injections was reported in case of WSe$_2$ using van der Waals (vdW) contacts of two-dimensional (2D) materials: graphite for an n-type contact and NbSe$_2$ for a p-type contact. Instead of conventional methods such as the evaporation of metals on TMD, 2D metals were transferred onto WSe$_2$ in order to form van der Waals contacts. These contacts showed a small Schottky barrier height for both carrier polarities. These finding revealed the potential of a high-performance vdW metal/ semiconductor contact for use in electronics applications.[37]

To overcome existing limitations in sensitivity and cost of state-of-the-art systems having high-sensitivity photo detection covering a large spectral range from the UV to IR is dominated by photodiodes, new device architectures and material systems are needed with low-cost fabrication and high performance. In the perspective of using low dimensional materials, the physical mechanism of photo-FETs (field-effect transistors) was described with recent advances in the field of low-dimensional photo-FETs and hybrids. The requirements of the channel material were addressed in view of the photon absorption and carrier transport process, and a fundamental trade-off between them was pointed out for single-material-based devices. It was also clarified how hybrid devices, consisting of an ultrathin channel sensitized with strongly absorbing semiconductors, can circumvent these limitations and lead to a new generation of highly sensitive photo detectors. Recent advances in the development of sensitized low-dimensional photo-FETs were discussed along with several promising future directions for their application in high-sensitivity photo detection.[38] The extensive energy band calculation schemes fail to reproduce the observed SBHs in 2D MoS$_2$-Sc interface. An ab initio quantum transport device simulation better reproduces the observed SBH in 2D MoS$_2$-Sc interface and highlights the importance of a higher level theoretical approach beyond the energy band calculation in the interface study. BL MoS$_2$-metal contacts generally have a reduced SBH than ML MoS$_2$-metal contacts due to the interlayer coupling and thus have higher electron injection efficiency. A theoretical study was conducted comparing the interfacial properties of monolayer and bilayer MoS$_2$ on Sc, Ti, Ag, Pt, Ni, and Au by using different theoretical models. Comparing the calculated and observed Schottky barrier heights suggested that many-electron effects are strongly depressed and the transport gap of a device depends on the DFT-GGA rather than the quasi particle band gap. Such a depression of many-electron effects can be applied to a general metal-2D semiconductor interface. In generally, the Schottky barrier heights are decreased from ML MoS$_2$-metal interfaces to BL MoS$_2$-metal interfaces due to the interlayer coupling, implying that BL MoS$_2$ with a higher electron injection efficiency is probably more suitable for a transistor than ML MoS$_2$ given the same gate controllability.[39] The problem in the understanding of the metal-2D semiconductor interface primarily comes from the anisotropy of the in-plane and out-of-plane electrical conductivity of the 2D-semiconductor. In-plane conductivity is almost two orders of magnitude higher than the out-of-plane conduction, which may severely affect the charge transport into the 2D semiconductors. For studying the importance of these two conductivity components two different device structures were fabricated using metal/MoS2 contact - one with Pd/MoS$_2$ Schottky junction and the other with Pd/MoS$_2$/Si heterojunction.[40]

Edge Contacts

Device and circuit fabrication technology of harvesting very high charge carrier mobility in 2D-Electron/Hole gases (2DEGs/2DHGs), realized in bulk semiconductor based heterojunctions have already been put to use in recent past in producing high electron mobility transistors (HEMTs) for commercial applications in connection with micro and millimeter wave frequency devices extensively. In these devices a thin sheet of 2DEG/2DHG are sandwiched between two higher band gap materials on either side constraining the charge carriers longitudinally but allowing them to move in transverse plane without any lattice scattering. Ohmic contacts to these 2DEG/2DHG sheets are made through their edges.[1,41–43] It is interesting to note that a similar scheme could possibly be used for making contacts to 2D-materials as reported recently.[44] Making ohmic contact to a 2D semiconductor in general has two options namely – one is to deposit metal onto the extended surface and other onto the edges according to HEMT metallization scheme.

In case of metal deposition on surface, particularly the non availability of surface bonding sites to establish chemical bonding through orbital hybridization results, in general, large contact resistance across planar metal and graphene monolayer interface.[45–52] For exploring edge contact metallization, the graphene sheet must be encapsulated in the form of h-BN/graphene/h-BN hetero structures (BN-G-BN) assembled for providing access to the graphene edges during metallization. Using conventional lithography to pattern and expose graphene surface is not favored practically as the resins used are difficult to remove, besides their presence degrades the electrical contact, channel mobility, adding contaminations across the interface, causing bubbles and wrinkles that multiply with the addition of each successive layer, limiting typical device size to ~1mm.[53–59] A novel technique described recently succeeded in realizing edge contact to the graphene layer by encapsulating in form of a stack of h-BN and graphene in BN-G-BN configuration. A hard mask of hydrogen-silsesquioxane (HSQ) resist applied onto the top BN surface of the stack allowed plasma etching to expose the edge. A composition of three metal layers (1 nm Cr, 15 nm Pd, and 60 nm Au) was e-beam deposited to establish electrical contact along the edge.[44] While characterizing this 1D contact, carrier injection limited to 1D atomic edge could reduce the contact resistance significantly low (~100ohm.mm). The fabricated graphene devices exhibited room-temperature mobility up to 140,000 cm^2/Vs and sheet resistivity below 40ohms/square at n>4×10^{12}/cm^2, approaching the theoretical limit due to acoustic phonon scattering. At temperatures below 40 K, a ballistic transport was observed over 15mm length scales.[44,47,52,60–62] The STEM image did not show any metal diffusion into the graphene/BN interface, confirming the edge nature of the contact. The EELS map additionally indicated that the contact was based on Cr adhesion layer. The extensive measurements of contact resistances was found scaling inversely with the contact width, and is largely independent of temperature in contrast to the linear temperature scaling reported for surface contacts.[44,48]

Recent Progress

Some recent experimental results reported in different laboratories are summarized here to highlight the situation regarding low contact fabrication of devices using 2D materials. Ideal electrical contacts to 2D-monolayers would ideally need similarly thin electrode materials while maintaining low contact resistances. A scalable method was reported for fabricating edge ohmic contacts to monolayer MoS_2 and WS_2 using graphene. The graphene and TMD layer were connected laterally with wafer-scale homogeneity, with no overlap or gap, and low average contact resistance of 30kΩ·µm showing linear *I–V* characteristics at room temperature maintaining down to liquid helium temperatures.[63] The intrinsic large band gap of MoS_2 limits its application in IR detection beside its high mobility, low off-state current and high on/off ratio. A high-performance IR photo detector was reported employing non-layers PbS and layered MoS_2 nanostructures via van der Waals epitaxy. DFT calculations indicate that PbS nano plates are in contact with MoS_2 edges through strong chemical hybridization, which offers enhanced response speed. The phototransistor exhibited a fast response ($\tau_{rising} = \tau_{decay}$ =7.8ms) as well as high photo responsively~4.5×10^4 A/W, and I_{light}/I_{dark}~1.3×10^2 in the near-IR region at room temperature with 3×10^{13} Jones detectivity, which was even better than that of commercial Si and In GaAs photo detectors. Furthermore, by controlling the growth and micro fabrication patterning, periodic device arrays of PbS–MoS_2 were capable of IR detection achieved on Si/SiO$_2$ substrates.[64] Currently employing few-layer graphene was demonstrated as a self-aligned edge-contacting scheme for layered material systems to take care of large contact resistance due to weak inter-layer coupling while circumventing the tunneling resistances of the weak coupling between layers.[65] A novel approach of forming low-resistance contacts to MoS_2 transistors with the intrinsic performance of the channel was reported a dry transfer technique and a metal-catalyzed graphene treatment process, nickel-etched-graphene electrodes were fabricated on MoS_2 showing contact resistance ~ 200Ω.µm. The fabrication of a clean graphene-MoS_2 interface and a low resistance nickel-graphene interface is critical for experimental low contact resistance.[66] The scaling of MoS_2 devices and contacts was examined with varying electrode metals and controlled deposition conditions, over a wide range of temperatures (80 to 500K), carrier densities (10^{12} to 10^{13}/cm^2), and contact dimensions (20 to 500nm). It was found that Au deposited in ultra-high vacuum (10^{-9}Torr) yielded three times lower R_C than under normal conditions, reaching 740Ω·µm and specific contact resistivity 3×10^{-7}Ω.cm^2, stable for over four months. The contact transfer length was 35nm at 300 K, as verified experimentally using devices with 20 nm contacts and 70 nm contact pitch (CP), equivalent to the '14 nm' technology node.[67]

Discussion

Taking a hint from the observation mentioned in the text it seems graphene monolayer is necessary to insert between 2D-semiconductor and metal for which a detailed theoretical modeling followed by appropriate technology seems to be necessary to develop. For minimizing the disturbances caused to the monolayer graphene from the presence of metal layer may be possibly designed using multiple layers of metal using atomic layer epitaxy (ALE). Similarly inserting something similar to h-BN monolayer should control the influence of multiple layers of 2D-semiconductor lying below. Besides, some species like O$_2$ or other may be attached to the interface to provide better stability and control.

Conclusion

Theoretical and experimental observations made so far give a strong evidence of realizing improved 2D-semiconductor based devices using graphene monolayer sheet in combination with a set of metal thin films in near future. Exploring planar and edge contacts with overhanging metal layer may be a better choice than any one technique alone. Use of ionic liquid and h-BN offers another possibility as mentioned in the text.

Acknowledgements

None.

Conflict of interest

The author declares no conflict of interest.

References

1. Ahmad S. Micro and Millimeter Wave Semiconductor Device Technology. Tata McGraw Hill: India; 1998.

2. Allain A, Kang J, Banerjee K, et al. Electrical contacts to two-dimensional semiconductors. *Nature Materials*. 2015;14:1195–1205.

3. Lopez Sanchez O, Lembke D, Kayci M, et al. Ultrasensitive photo detectors based on monolayer MoS2. Nature Nanotech. 2013;8:497–501.

4. Krasnozhon D, Lembke D, Nyffeler C, et al. MoS$_2$ transistors operating at gigahertz frequencies. *Nano Lett*. 2014;14(10):5905–5911.

5. Das S, Chen HY, Penumatcha AV, et al. High performance multilayer MoS$_2$ transistors with scandium contacts. *Nano Lett*. 2013;13(1):100–105.

6. Liu H, Neal AT, Ye PD. Channel length scaling of MoS$_2$ MOSFETs. *ACS Nano*. 2012;6(10):8563–8569.

7. Liu H, Si M, Najmaei S, et al. Statistical study of deep submicron dual-gated field-effect transistors on monolayer chemical vapor deposition molybdenum disulfide films. *Nano Lett*. 2013;13(6):2640–2646.

8. Landauer R. Spatial variation of currents and fields due to localized scatterers in metallic conduction. *IBM J Res Dev*. 1957;1:223–231.

9. Sharvin YV. A possible method for studying Fermi surfaces. *Sov Phys JETP*. 1965;21(3):655–656.

10. Jena D, Banerjee K, Xing GH. 2D crystal semiconductors: Intimate contacts. *Nat Mater*. 2014;13(12):1076–1078.

11. Wright GT. Small-signal theory of the transistor transit-time oscillator (translator). *Solid-State Electronics*. 1979;22(4):399–403.

12. SM Sze. Physics of Semiconductor Devices. *Wiley Inter science*. 1969;832.

13. Bardeen J. Surface States and Rectification at a Metal Semi-Conductor Contact. *Phys Rev*. 1947;71:717.

14. Xu Y, Cheng C, Du S, et al. Contacts between Two and Three-Dimensional Materials: Ohmic, Schottky, and *p*-n Hetero junctions. *ACS Nano*. 2016;10(5):4895–4919.

15. Das S, Chen HY, Penumatcha AV, et al. High-Performance Multilayer MoS2 Transistors with Scandium Contacts. *Nano Lett*. 2013;13(1):100–105.

16. Zhao Y, Xiao X, Huo Y, et al. Influence of Asymmetric Contact Form on Contact Resistance and Schottky Barrier, and Corresponding Applications of Diode. *ACS Appl. Mater. Interfaces*. 2017;9(22):18945–18955.

17. Kim KS, Kim KH, Nam Y, et al. Atomic Layer Etching Mechanism of MoS2 for Nano devices. *ACS Appl Mater Interfaces*. 2017;9(13):11967–11976.

18. Roy S, Neupane GP, Dhakal KP, et al. Observation of Charge Transfer in Heterostructures Composed of MoSe2Quantum Dots and a Monolayer of MoS2 or WSe2. *J Phys Chem C*. 2017;121(3):1997–2004.

19. Doan MH. Jin Y, Adhikari S, et al. Charge Transport in MoS2/WSe2 van der Waals Heterostructure with Tunable Inversion Layer. *ACS Nano*. 2017;11(4):3832–3840.

20. Ross JS, Rivera P, Schaibley J, et al. Interlayer Exciton Optoelectronics in a 2D Hetero structure p–n Junction. *Nano Lett*. 2017;17 (2):638–643.

21. Xu K, Chen D, Yang F, et al. Sub-10nm Nanopattern Architecture for 2D Material Field-Effect Transistors. *Nano Lett*. 2017;17 (2):1065–1070.

22. Kim C, Moon I, Lee D, et al. Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano*. 2017;11(2):1588–1596.

23. Guan J, Chuang HJ, Zhou Z, et al. Optimizing Charge Injection across Transition Metal Dichalcogenide Heterojunctions: Theory and Experiment. *ACS Nano*. 2017;1(4):3904–3910.

24. Zheng C, Zhang Q, Weber B, et al. Hellerstedt, Y. Zhang, W. H. Duan, Q. Bao, and M. S. Fuhrer. Direct Observation of 2D Electrostatics and Ohmic Contacts in Template-Grown Graphene/WS2 Heterostructures. *ACS Nano*. 2017;11(3):2785–2793.

25. Stradi D, Papior NR, Hansen O, et al. Field Effect in Graphene-Based van der Waals Heterostructures: Stacking Sequence Matters. *Nano Lett*. 2017;17(4):2660–2666.

26. Li L, Zhang L, Shi L, et al. MXene Ti3C2: An Effective 2D Light-to-Heat Conversion Material. *ACS Nano*. 2017;11(4):3752–3759.

27. Lin H, Wang X, Yu L, et al. Two-Dimensional Ultrathin MXene Ceramic Nanosheets for Photothermal Conversion. *Nano Lett*. 2017;17(1):384–391.

28. Huang L, Li B, Zhong M, et al. Tunable Schottky Barrier at MoSe2/Metal Interfaces with a Buffer Layer. *J Phys Chem C*. 2017;121(17):9305–9311.

29. Yoon Y, Ganapathi K, Salahuddin S. How Good Can Monolayer MoS2 Transistors Be? *Nano Lett*. 2011;11(9);3768–3773.

30. Wang H, Yu L, Lee YH, et al. Integrated Circuits Based on Bilayer MoS2 Transistors. *Nano Lett*. 2012;12(9):4674–4680.

31. Sattar S, Schwingenschlögl U. Electronic Properties of Graphene–PtSe2 Contacts. ACS Appl. Mater. Interfaces. 2017;9(18):15809–15813.

32. Kim HG, **Lee** HBR. Atomic Layer Deposition on 2D Materials. *Chem Mater*. 2017;29(9):3809–3826.

33. Nourbakhsh A, Zubair A, Sajjad RN, et al. MoS2 Field-Effect Transistor with Sub-10 nm Channel Length. *Nano Lett*. 2016;16(12):7798–7806.

34. Leong WS, Luo X, Li Y, et al. Low Resistance Metal Contacts to MoS2 Devices with Nickel-Etched-Graphene Electrodes. *ACS Nano*. 2015;9(1):869–877.

35. Chuang HJ, Chamlagain B, Koehler M, et al. Low-Resistance 2D/2D Ohmic Contacts: A Universal Approach to High-Performance WSe2, MoS2, and MoSe2 Transistors. *Nano Lett*. 2016;16(3):1896–1902.

36. Kim Y, Kim AR, Yang JH, et al. Alloyed 2D Metal–Semiconductor Heterojunctions: Origin of Interface States Reduction and Schottky Barrier Lowering. *Nano Lett*. 2016;16(9):5928–5933.

37. Sata Y, Moriya R, Masubuchi S, et al. N and P-type carrier injections into WSe$_2$ with van der Waals contacts of two-dimensional materials. *Jap J App Phys*. 2017.

38. Kufer D, Konstantatos G. Photo-FETs: Phototransistors Enabled by 2D and 0D Nanomaterials. *ACS Photonics*. 2016;3(12):2197–2210.

39. Zhong H, Quhe R, Wang Y, et al. Interfacial Properties of Monolayer and Bilayer MoS2 Contacts with Metals: Beyond the Energy Band Calculations. *Scientific Rep*. 2016.

40. Wong CPY, Troadec C, Goh KEJ. A Study of the Metal/2D Semiconductor Contacts.

41. Bin A, Khudhayr. Developing of Low-resistance Ohmic Contact on GaN HEMTs for High Operating Frequency Applications.

42. Taneja D, Sfigakis F, Croxall AF, et al. Ritchie. N-type ohmic contacts to undoped GaAs/AlGaAs quantum wells using only front-sided processing: application to ambipolar FETs. *Semicond Sci Technol*. 2016;31:1–7.

43. Parikh P, Wu Y, Shen L. Commercialization of high 600V GaN-on-silicon power HEMTs and diodes. *IEEE Energy Tech*. 2013:21–23.

44. Wang L, Meric I, Huang PY, et al. One-Dimensional Electrical Contact to a Two-Dimensional Material. *Science*. 2013;342:614–617.

45. Giovannetti G, Khomyakov PA, Brocks G, et al. Doping graphene with metal contacts. *Phys Rev Lett*. 2008;101.

46. Tang Q, Zhang CX, He C, et al. Charge transport properties of graphene: Effects of Cu-based gate electrode. *J Appl Phys*. 2010;108:123711.

47. Léonard F, Talin AA. Electrical contacts to one- and two-dimensional nanomaterials. *Nat Nanotechnol*. 2011;6:773–783.

48. Xia F, Perebeinos V, Lin YM, et al. The origins and limits of metal-graphene junction resistance. Nat Nanotechnol. 2011;6:179–184.

49. Choi MS, Lee SH, Yoo WJ. Plasma treatments to improve metal contacts in graphene field effect transistor. *J Appl Phys*. 2011;110:073305.

50. Berdebes D, Low T, Sui Y, et al. Lundstrom. Substrate Gating of Contact Resistance in Graphene Transistors. *IEEE Trans Electron Dev*. 2011;58:3925–3932.

51. Moon JS, Antcliffe M, Seo HC, et al. Ultra-low resistance ohmic contacts in graphene field effect transistors. *Appl Phys Lett*. 2012;100:203512.

52. Smith JT, Franklin AD, Farmer DB, et al. Reducing contact resistance in graphene devices through contact area patterning. *ACS Nano*. 2013;7:3661–3667.

53. Geim AK, Grigorieva IV. Van der Waals heterostructures. *Nature*. 2013;499:419–425.

54. Mayorov AS, Gorbachev RV, Morozov SV, et al. Micrometer-scale ballistic transport in encapsulated graphene at room temperature. *Nano Lett*. 2011;11:2396–2399.

55. Ishigami M, Chen JH, Cullen WG, et al. Atomic Structure of Graphene on SiO2. *Nano Lett*. 2017;7:1643–1648.

56. Robinson JA, LaBella M, Zhu M, et al. Contacting graphene. *Appl Phys Lett*. 2011;98:053103.

57. Yamaguchi J, Hayashi K, Sato S, et al. Passivating chemical vapor deposited graphene with metal oxides for transfer and transistor fabrication processes. *Appl Phys Lett*. 2013;102:143505.

58. Lindvall N, Kalabukhov A, Yurgens A. Erratum: "Cleaning graphene using atomic force microscope. *J Appl Phys*. 2012;111:064904.

59. Haigh SJ, Gholinia A, Jalil R, et al. Cross-sectional imaging of individual layers and buried interfaces of graphene-based hetero structures and super lattices. *Nat Mater*. 20102;11:764–767.

60. Matsuda Y, Deng WQ, Goddard WQ. Contact Resistance for "End-Contacted" Metal-Graphene and Metal-Nanotube Interfaces from Quantum Mechanics. *J Phys Chem C*. 2010;114(41):17845–17850.

61. Cho K. First-principles and quantum transport studies of metal–graphene end contacts. *MRS Proc*. 2010;1259:S14–S35.

62. Wu Y, Wang Y, Wang J, et al. Electrical transport across metal-two-dimensional carbon junctions: edge versus side contacts. *AIP Adv*. 2012;2(1):012132.

63. Guimarães MHD, Gao H, Han Y, et al. Atomically Thin Ohmic Edge Contacts Between Two-Dimensional Materials. *ACS Nano*. **2016**;10(6):6392–6399.

64. Wen Y, Yin L, He P, et al. Integrated High-Performance Infrared Phototransistor Arrays Composed of Nonlayered PbS–MoS2 Heterostructures with Edge Contacts. *Nano Lett*. **2016**;16(10):6437–6444.

65. Chu T, Chen Z. Understanding the Electrical Impact of Edge Contacts in Few-Layer Graphene. *ACS Nano*. **2014**;8(4):3584–3589.

66. Leong WS, Luo X, Li Y, et al. Low Resistance Metal Contacts to MoS2 Devices with Nickel-Etched-Graphene Electrodes. *ACS Nano*. 2015;9(1):869–877.

67. English CD, Shine G, Dorgan VE, et al. Improved Contacts to MoS2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett*. **2016**;16(6):3824–3830.