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Recent trend in high-speed wireline link design

Abstract

This short article provides a brief summary of the current status of high speed wireline links and its future trend. It also captures the motivating factors for recent changes and explains the fundamental reasons behind it. Lower SNR in multilevel modulation has motivated recent change in the link architecture developed in leading R & D groups and differentiating features. Lastly, it points out the challenges to motivate future research work in academia and industry.

Keywords: wireline, inter-symbol-interference, modulationt

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Abbreviations: ISI, inter symbol interference; CTLE, continuous time linear equalization; DFE, decision feedback equalization; FFE, feed-forward equalization

The need for speed

We are at a historical cross road in technology roadmap where the numbers of objects connected through internet have vastly outnumbered the human network. This network of smart objects, also known as IoT, will shape our life in the next decade and beyond. By 2020, the number of smart objects is expected to reach 100 million sending massive information over internet. To accommodate such user demand, data centers are also evolving both electrical and optical links are adopting complex modulation schemes. Eventually the need for higher speed from the users, service provider and equipment manufacturer motivates the researchers to push the limit of semiconductor device physics and communication theory. Ultimately, the end product is a fully integrated monolithic solution capable of transmitting and receiving terabits of information. Few example of such market driven R & D development efforts are given in Figure 1. While the particular development trend in each company may vary based on their business strategy, one consistent trend is the rapid increase in data rate over time. Figure also includes example work from these efforts and that also capture underline motivating factors:

a) All of them are designed for massive parallel interface, with clear indication that we need to achieve higher individual link speed as well as high density to aggregate higher information exchange rate.

b) Beyond 40 Gb/s almost everyone is converging to higher order (PAM-4) modulation.

c) All these transceivers are built in leading nodes in CMOS technology as continuation of Moore's law.

Over last two decades wire-line channels have evolved drastically to overcome high frequency losses. High frequency loss causes the transmitted symbols to disperse which results in inter-symbol-interference (ISI). The techniques to reduce these ISI components are known as equalization. The recent advances in interconnect technology and development of low loss dielectric such as Megatron have significantly extended their reach. This improvement in channel along with advances in equalization techniques have enables 100 Gb/s Ethernet. Improving the loss characteristics of channel increases system cost as shown in Figure 2. However, industry is facing an inevitable challenge despite using expensive lowest loss material and high quality connectors, only few 10s of cm channels suffering 45 dBs of loss @ 25GHz. Such channel loss causes significant inter symbol interference (ISI), and existing equalization techniques are proving to be insufficient to compensate that. Unfortunately, this also aligns with the end of Moore's law; therefore, we can no longer rely on higher performance devices to overcome the challenges. This creates an opportunity for disruptive technology and architecture.

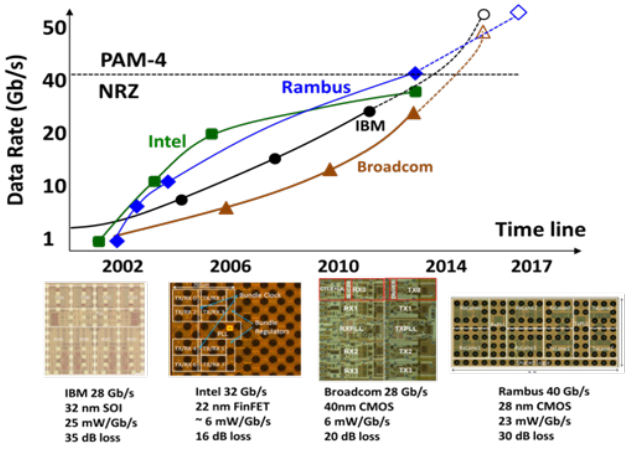

Figure 1 Trend in High speed Link development in leading research and development groups in the world. Below is the example demonstration developed hardware solution with performance summary.

How well can we equalize?

In high-speed wireline transceivers, the frequency dependent channel loss is the main source of inter-symbol interference (ISI). In simple word, ISI is the residue of the current symbol that affects the following symbols (pre-cursor) as well as the previous symbols (post-cursor). For high loss channel, conventional receiver designs usually feature analog linear equalization techniques such as continuous time linear equalization (CTLE) and passive equalization at the front end as shown in Figure 3. In addition, decision feedback equalization (DFE) and feed-forward equalization (FFE) techniques are used for further ISI cancellation and bit detection. Fundamentally, this limitation is coming from degradation of low signal-to-noise and signal-to-crosstalk ratio that is unavoidable in existing equalization techniques. Analog mixed-signal solution in general can equalize with excellent energy efficiency (around ~3pJ/bit.[1] But these solutions

have their limitations: first, SNR degradation CTLE that generally inverts the channel also amplifies noise, including crosstalk noise and degrades SNR. Second, the linearity requirement scaled supply reduces maximum achievable linear swing. Third, process variation makes it very difficult to achieve reliable control over zero and pole frequencies to achieve the desirable frequency response. All these factors limit the performance of existing equalization techniques and ultimately our demonstrated capability of equalization is limited to 40 dB (Figure 4).

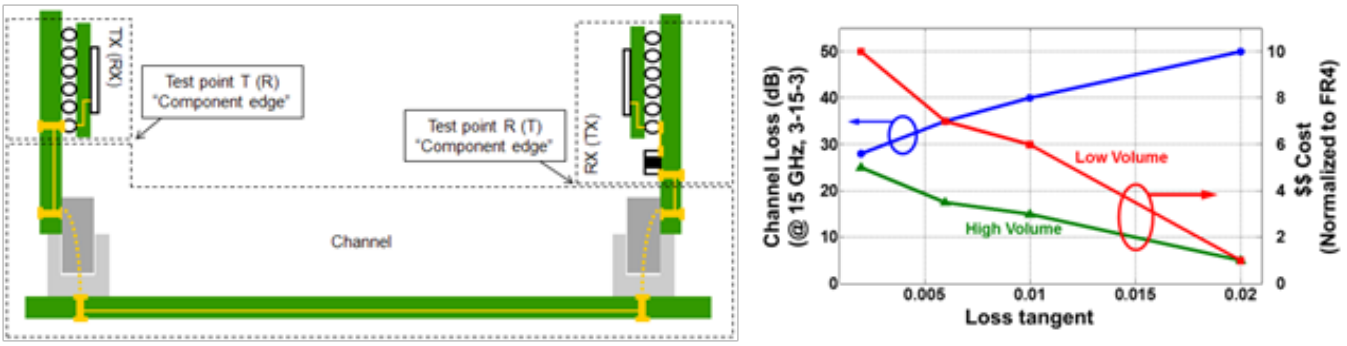

Figure 2 Example of a typical back plane channel and its loss and cost as a function of loss tangent.

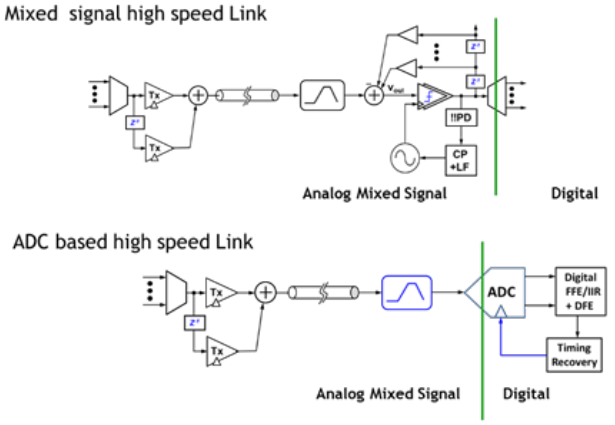

Figure 3 Conventional Analog mixed signal links and ADC based links.

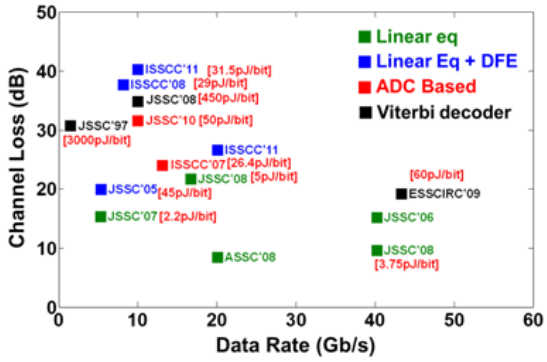

Figure 4 Trend in Equalization techniques at different data rates and channel loss.

To digitize or not to digitize?

The equalization becomes more complicated when we move to higher order modulation as PAM-4 for several reasons

a) Compared to binary/PAM-2 signaling, the eye height reduces by 3x for the same transmit power - this translates to 9 dB SNR penalty and corresponding BER degradation.

b) Linearity requirement for PAM-4 signaling is much more stringent, that makes analog processing much more challenging compared to NRZ signaling although the supply is scaling with technology.

c) Residue ISI has much bigger impact in PAM-4 compared to NRZ. This is because residue of the largest transition impacts the smallest bit both as ISI and crosstalk that is 3x larger compared to NRZ.[2–5]

All these challenges motivate us to rethink the equalization strategy as well as receiver architecture. Recently ADC based architectures are gathering interest to enhance performance through digital processing. Therefore, in ADC based receivers where equalization is done digitally, can take advantage of the technology scaling, enables advanced equalization that can compensate higher loss compared to traditional mixed signal equalization. However, the challenge in this architecture is the front-end ADC that consumes significant power to provide the required resolution. When compared to traditional mixed signal receiver, ADC based solutions' power consumption is 2x higher.[6–13] Fortunately, recent trend is to improve their energy efficiency significantly, most of those are enabled through academic research and development that allows flexibility for disruptive approaches (Figure 5). Given the strict energy efficiency target, application of ADC based links depends on successful adoption of these techniques.

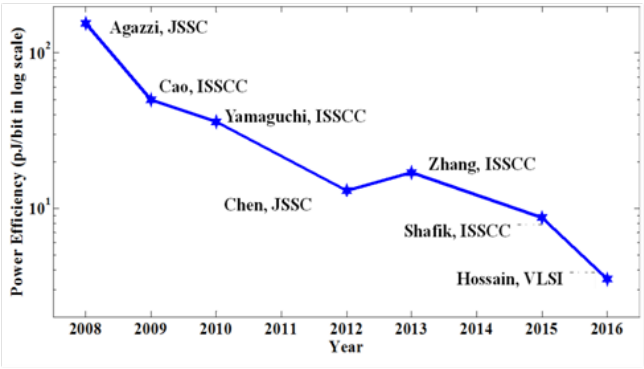

Figure 5 Energy efficiency trend in ADC based links for wireline communication.

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Conflict of interest

The author declares no conflict of interest.

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