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High speed comparator based switched capacitor integrator based on non linear current source

Abstract

A new structure for comparator-based switched-capacitor integrator (CBSCI) is presented. This structure increases the clock frequency considerably by using a non-linear current source. The proposed integrator involves replacing the two linear current sources in conventional CBSCI with just one non-linear current source. Also new logic part is presented which reduces the circuit size and power dissipation consequently. According to proposed structure, a first order CBSCI is designed in 0.18µm CMOS technology with a 100MHz clock frequency.

Keywords: comparator-based switched-capacitor, integrator, non-linear current source

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Introduction

Most of switched-capacitor based circuits use operational amplifiers (OPAMP) for utilization and OPAMP gain is the most important criterion for the accuracy of these kinds of circuits.[1] While the scaling down of supply voltage and channel length of CMOS technology limit the design procedure. Gain and voltage swing are the main problems which both have been reduced. So finding an alternative for OPAMPs is a possible strategy to avoid imposed restrictions by advancement of CMOS technology. Comparator-Based Switched-Capacitor circuits are kinds of circuits which have removed OPAMP and instead of it use a comparator and current sources. These circuits have shown higher power efficiency and are unconditionally stable due to removed feedback. The most valuable feature of an OPAMP is the virtual ground effect that should be simulated in CBSCC to perform proper operations. In fact virtual ground detection for inputs of comparator is the major concentration in these circuits. This can be realized by extra circuit which includes current sources and logic control part. Some techniques have introduced to reduce the CBSCC delay issue. Lower common mode voltage for comparator inputs, using two comparators, common mode feedback, common mode feed forward, using an extra clock and overshoot correction circuit are presented in.[1,3–14] All the above techniques have failed to reduce delay time considerably or have designed in complicated extra circuitry. In this paper we have proposed a new technique to faster detection of virtual ground effect. New schemes for current sources and logic control part are explained and we have used this technique to design a CBSCI. This integrator can use to form a Sigma-Delta Modulator (SDM) which is the most important part of a Sigma-Delta analog to digital convertor.

Conventional CBSCI

The conventional CBSCI has shown in (Figure 1) consists of a comparator followed by a logic unit which generates control signals as E1 (coarse charge transfer), E2 (fine charge transfer), S (output switch), and P (preset switch).[15] E1 and E2 are applied to two linear current sources, I1 and I2 which charge and discharge the load capacitor as coarse and fine charge transfer. The timeline of this integrator has shown in (Figure 2). According to (Figure 2) during the sampling phase the input signal has sampled in Cs and charge transfer phase begin with rising Φ2. In the beginning of this phase a preset pulse is applied to the output, connecting it to the lowest voltage in the circuit. Then a coarse charge transfer phase E1 and a fine charge transfer phase E2 charge and discharge the load capacitor respectively in order to creation of virtual ground effect. During the preset phase, the virtual ground node (the comparator positive input), Vx, drop below the common-mode voltage, Vcm, and resetting the comparator. The logic control part raises E1, and I1 charges the load capacitor (output node) up to the virtual ground node equals the common-mode voltage (coarse charge transfer). At this time, the comparator set, however the load capacitor has charged up higher than proper value due to the comparator delay time. So an overshoot error has produced which shown in (Figure 2). In order to correction extra charges the logic control part pull down the E1 and raises the E2 which cause to discharges the output node by I2 (fine charge transfer) which has slower rate compared with I1, until the virtual ground node voltage becomes lower than Vx, at this time the output of comparator resets again and both of E1 and E2 are came down. Here, switch S opens by logic control part and the correct value is sampled on the load capacitor (which is the sampling capacitor of the next stage).[16] The output is slightly lower than the ideal value because of the comparator delay time. This delay time produces a constant signal-independent undershoot each cycle which shown in (Figure 2). In fact we need to reach the correct output value only at the sampling instant and it doesn't matter how it reaches there. By this procedure we are able to detect the virtual ground effect in order to removing the OPAMPs.[17] This strategy helps us to abandon issues of speed, gain, and stability. Replacing the OPAMP with comparator also has significant effect to power consumption issues due to lower power dissipation of comparators in comparison to OPAMPs.[18]

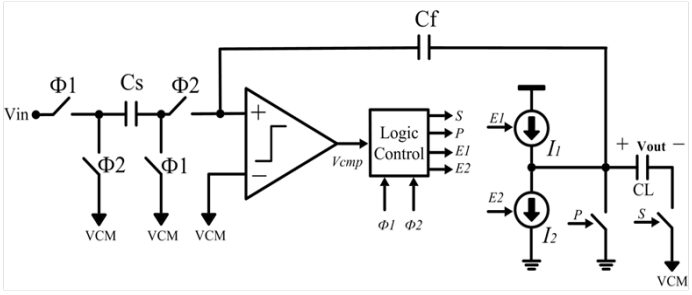

Figure 1 Schematic of Conventional CBSCI.

Proposed CBSCI

The proposed CBSCI has shown in (Figure 3) which consists of sampling circuit, a comparator, a simple logic control part and a

non-linear current source. The sampling circuit operates exactly like opamp-based switch capacitor circuit which sample the input signal and hold it for charge transfer phase, also logic control part include just three simple logic gates as three inputs and two inputs ANDs and an inverter. This logic control part is specified by red rectangular in (Figure 3). Also the main important part of this circuit is non-linear current source. This current source specified by green rectangular in (Figure 3), uses the M1 and M2 as switch and a PMOS transistor to drive large current as M5. Time line of this integrator has shown in (Figure 4) which shows logic signals and non-linear charging for virtual ground creation. According to (Figure 4) this circuit works in two main phases, the sampling phase and the charge transfer phase. In addition the charge transfer phase consists of two sub phases, the preset phase and the charge phase. During Φ1, the input signal is sampled and Φ2 begin with preset phase like conventional circuit and following the unique charge phase begins, which at the end of this sub phase S switch opens so the integration is performed. This integrator can operate with higher clock frequency due to unique charge phase.[19] Also the logic part is miniaturized in compare with conventional circuit which reduces the circuit size and power consumption consequently. After sampling phase and in the beginning of Φ2, the P switch closes and output node connects to ground (the minimum voltage in the circuit). This cause the Vx becomes lower than Vcm so the comparator output set to high (inputs of comparator in proposed circuit are vice versa in comparison to conventional CBSCI). At this time outputs of ANDs, S and E are high and low respectively so the S switch is close and the gates of M1 and M2 are in low voltage which makes M1 off and M2 on considering that M1 is a NMOS and M2 is a PMOS transistor. So the gate of M4 as a PMOS type connects to supply voltage which makes it off and as a result the current mirror is off. In this condition M5 don't charge the output node. Time of preset phase depends on capacitors connected to output node. In fact the preset phase is the appropriate time to discharge output node in order to reduce the Vx to lower voltage value than Vcm. This causes the value of Vx to go below the Vcm and consequently the output of the comparator is set to high. The next step is charge phase which has the most difference in this work in compare to other works. In this phase E and S is high so S switch is close and non-linear current source is working. The gates of M1 and M2 have high voltage so M1 is on and M2 is off. The gate of M4 connected to Vx which has lower value than Vcm at the beginning. So M4 is in triode region and has a current like (1).

$$\left|I_{d4}\right| = \mu_p C_{ox} \left(\frac{W}{L}\right)_4 \left(V_{GS} - V_{thp}\right) V_{ds} - \frac{1}{2} V_{ds}^2 \qquad (1)$$

This current passes through M3 and copies to M5 and even can be amplify with current mirror gain. Finally the M5 charge output node by current which is proportional to Vx. This procedure charges the output node and Vx node consequently by through Cf. As the voltage of Vx is raising the source-gate voltage of M4 is falling so the current of M4 and M5 decrease respectively this can be cause changing in operation for M4 from triode to saturation and current can expresses by (2).

$$\left|I_{d4}\right| = \frac{1}{2} \mu_p C_{Ox} \left(\frac{W}{L}\right)_4 \left(V_{GS} - V_{thp}\right)^2 \left(1 + \lambda V_{ds}\right) \qquad (2)$$

Again by charging, the Vx increases and the current of M5 decreases, so a non-linear charging system creates. This non-linear charging continues the raising Vx voltage to the point that Vx reaches above than Vcm which changes the comparator output state. At this time the comparator output sets to low and current source is off and the S switch is open. So the charge transfer phase is completed. The comparator used in this circuit plays an important role to logic part stimulation. This comparator must have high speed and high resolution in order to be efficiently applicable in the proposed CBSCI at high clock frequency. The selected comparator in the proposed circuit shown in (Figure 5) includes three major part: source-coupled differential pair with positive feedback specified by red rectangular, differential to single-ended converter specified by green rectangular and output buffer specified by blue rectangular. The first part provides high resolution due to positive feedback. Also the differential to single-ended improves the gain of first part and finally the output buffer complete output node voltage swing.

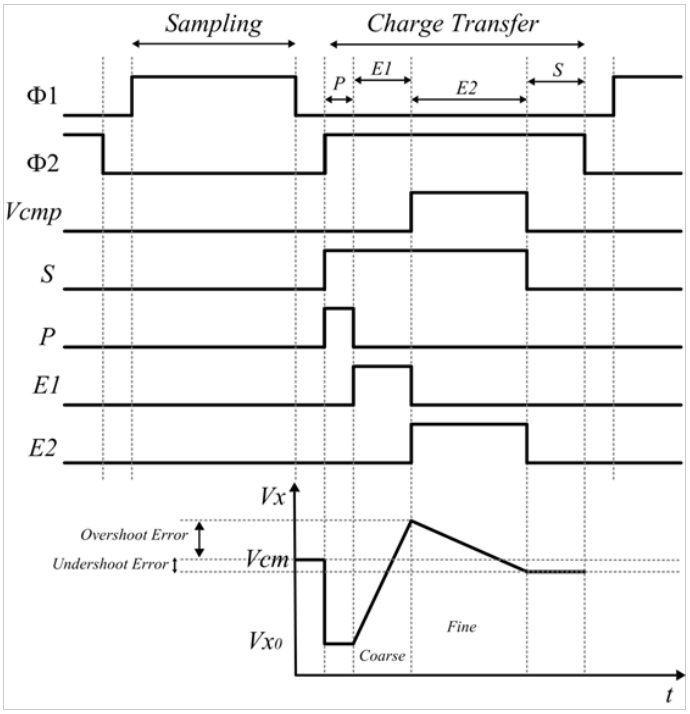

Figure 2 Time line of Conventional CBSCI.

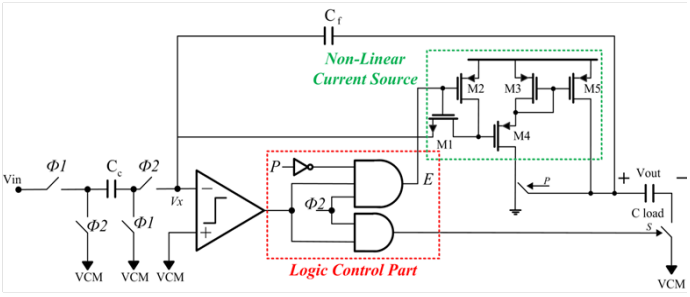

Figure 3 Schematic of Proposed CBSCI with non-linear current source.

Simulation Results

We designed proposed CBSC integrator in standard 0.18µm CMOS (Table 1) process and biased it with a 1.8V power supply voltage.[20] Non-overlapped clock frequencies, i.e. Φ1 and Φ2, choose 100MHz. Also input signal is a sinusoidal wave, has 1MHz frequency

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and 50mV amplitude. The sampling, feedback and load capacitor are 1pF, 4pF and 2pF respectively. (Figure 6) shows the input and output signals of proposed CBSC integrator with 100MHz clock frequency.[21] In addition (Table 2) is presented to show the output phase in different sampling and input frequencies. To insure the accuracy of the proposed integrator we should check the Vx voltage and control signals which have been shown in (Figure 7). In this integrator comparator output trigger the non-linear current source and logic control part. Also the output of comparator depends on Vx as shown in (Figure 7). So in charge transfer phase when Vx is lower than common mode voltage (in this circuit selected equal to 0.65V) the comparator output is high and non-linear current source is working in order to charging output node and raising Vx respectively.[22] when the Vx voltage be greater than common mode voltage, the comparator output set to low, non-linear current source is off and S switch opens as shown in (Figure 7).

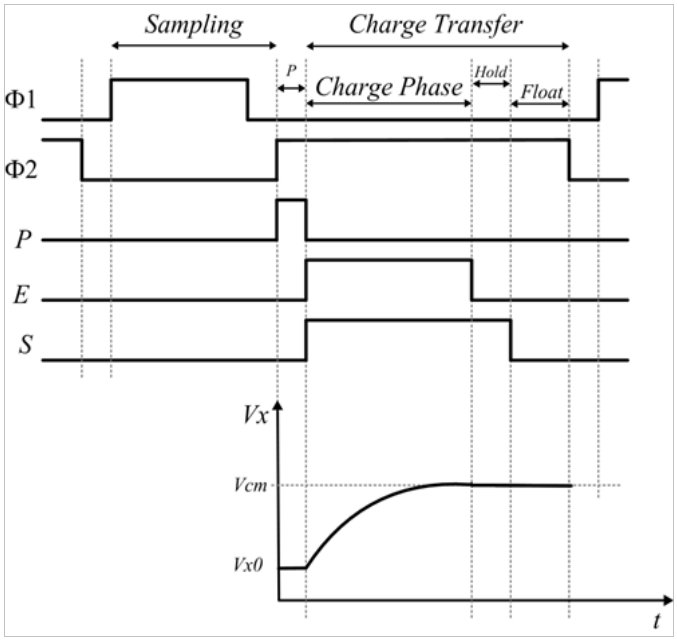

Figure 4 Time line of Proposed Integrator.

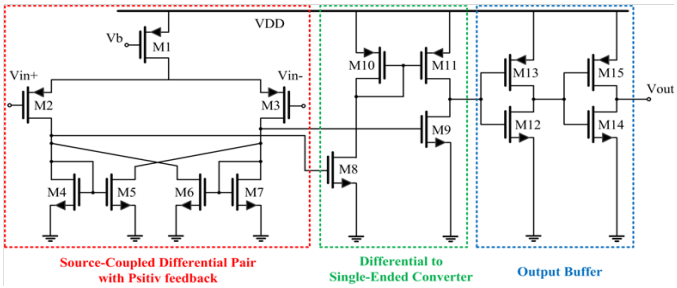

Figure 5 Schematic of utilized comparator.

Finally, (Table 3) shows the clock frequency and overshoots cancellation technique comparison between this work and previous works presented in literature. According to (Table 2) proposed integrator has higher clock frequency by using non-linear current source and simple logic part. In addition (Figure 8) shows the frequency spectral of output signal.[23]

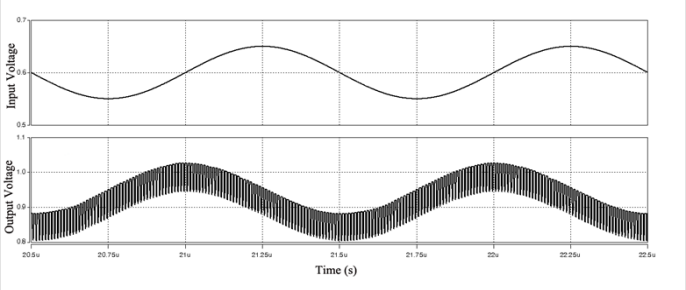

Figure 6 Input and output signals of proposed CBSC integrator in 100MHz clock frequency.

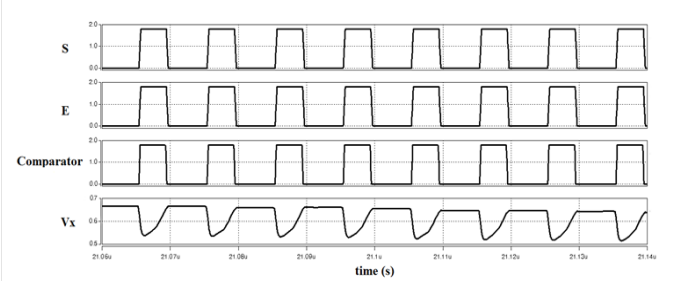

Figure 7 Vx and Control signals.

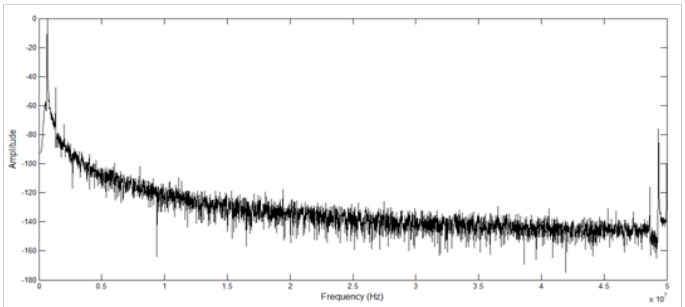

Figure 8 Frequency spectral of output signal.

Table 1 Transistor sizing of current source and comparator

Current source		**Comparator**	
Transistor	Dimension	Transistor	Dimension
M1	0.22μm/0.18μm	M1	4.5μm/0.18μm
M2	0.22μm/0.18μm	M2, M3,M8	1.8μm/0.18μm
M3	50μm/0.18μm	M4, M7	0.54μm/0.18μm
M4	50μm/0.18μm	M5, M6, M10, M11	0.36μm/0.18μm
M5	60μm/0.18μm	M9	2.7μm/0.18μm

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Table 2 Output phase in different frequencies

Sampling frequency	Input frequency	Output phase
12.5MHz	125KHz	89.4°
25MHz	250KHz	89.1°
50MHz	500KHz	88.7°
100MHz	1MHz	88.4°

Table 3 Output phase in corner cases for 100MHz clock frequency

Corner case	Output phase
SS	87.3
SF	87.7
FS	87.6
FF	88.1

Table 4 Clock frequency comparison

Reference	Technology	VDD	Topology	Overshoot cancellation technique	Clock frequency
1	0.18µm CMOS	1.8V	Pipeline ADC	Lower common mode voltage	7.9MHz
2	0.18µm CMOS	1.8V	Pipeline ADC	Using two comparators	20MHz
3	0.18µm CMOS	1.8V	Pipeline ADC	Extra clock in logic	40MHz
4	0.18µm CMOS	1.8V	Pipeline ADC	Overshoot correction circuit	10MHz
5	0.18µm CMOS	1.8V	5th Single-Loop ΣΔ ADC	Overshoot correction circuit	32MHz
This work	0.18µm CMOS	1.8V	Integrator	Non-linear current source	100MHz

Conclusion

A new structure for CBSC integrator has presented in this paper. Increasing the clock frequency was the major achievement, obtained by using a non-linear current source. Also a new logic part has introduced which is less complex in compare to previous works. The proposed integrator simulated in standard 0.18µm CMOS process and biased with a 1.8V power supply voltage with 100MHz clock frequency.[24,25]

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None.

Conflict of interest

The author declares no conflict of interest.

References

1. Fiorenza JK, Sepke T, Holloway P, et al. Comparator-based switched-capacitor circuits for scaled CMOS technologies*IEEE Journal of Solid-State Circuits*. 2006;41(12):2658–2668.
2. Zamani M, Jafarabadi Ashtiani S, Dousti M, et al. A10b, 20-MS/s, 2.6mW fully differential CBSC pipelined ADC in 0.18.MU. m CMOS. *IEICE Electronics Express*. 2010;7(23):1694–1701.
3. Zamani M, Jafarabadi Ashtiani S, Dousti M. A12b, 40-MS/s, 4.1mW fully differential CBSC pipelined ADC in 0.18. MU. m CMOS. *IEICE Electronics Express*. 2010;7(23):1714–1720.
4. Huang MC, Liu SI. A 10-MS/s-to-100-kS/s power-scalable fully differential CBSC 10-bit pipelined ADC with adaptive biasing. *IEEE Transactions on Circuits and Systems II: Express Briefs*. 2010;57(1):11–15.
5. Zamani M, Taghizadeh M, Moghadasi MN, et al. A 5th-order ΣΔ modulator with combination of op-Amp and CBSC circuit for ADSL applications. *Analog Integrated Circuits and Signal Processing*. 2012;71(1):143–150.
6. Wong KF, Sin SW, Seng Pan U, et al. A modified charging algorithm for comparator-based switched-capacitor circuits. 52nd IEEE International Midwest Symposium; 2009 Aug 2-5; Cancun, Mexico: IEEE; 2009.
7. Mortazavi SY, Nabavi A, Amiri P. High-accuracy Comparator-Based Switched-Capacitor structure. *IEICE Electronics Express*. 2010;7(5):352–359.
8. Parsan FA, Ayatollahi A. A comparator-based switched-capacitor integrator using a new charge control circuit. In *SOC Conference;* Sept 17–20; CA,USA: IEEE; 2008.
9. Wulff C, Ytterdal T. Comparator-based switched-capacitor pipelined analog-to-digital converter with comparator preset, and comparator delay compensation. *Analog Integrated Circuits and Signal Processing*. 2011;67(1):31–40.
10. Chae J, Temes GC. Comparator-based buffer with resistive error correction. *Electronics letters*. 2010;46(17):1188–1190.
11. Wong KF, Sin SW, Seng Pan U, et al. Level-Shifting variable current charging technique for high-speed Comparator-Based Switched-Capacitor circuits. 53rd IEEE International Midwest Symposium; Aug 1-4; Seattle, USA: IEEE; 2010.
12. Rajaee O, Maghari N, Moon UK. Time-Shifted CDS Enhancement of Comparator-Based MDAC for Pipelined ADC Applications. 14th IEEE International Conference on Electronics, Circuits and Systems; Dec 11-14; Marrakech, Morocco: IEEE; 2007.
13. Ding L, Chan S, Wong KF, et al. A pseudo-differential comparator-based pipelined ADC with common mode feed forward technique. APCCAS 2008 IEEE Asia Pacific Conference on Circuits and Systems; 2008 Nov 30- Dec 3 Macao, China: IEEE; 2009.
14. Musah T, Kwon S, Lakdawala H, et al. A 630µW zero-crossing-based ΔΣ ADC using switched-resistor current sources in 45nm CMOS. 2009 IEEE Custom Integrated Circuits Conference; Sept 13-16. Rome, Italy: IEEE; 2009.
15. Largani, Hosseini, Sajid, et al. A new frequency compensation technique for three stages OTA by differential feedback path. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*. 2014;28(4):381–388.

16. Biabanifard Sadegh, Meysam Akbari, Mehdi Largani, et al. High performance reversed nested Miller frequency compensation. *Analog Integrated Circuits and Signal Processing*. 2015;85(1):223–233.
17. Shahsavari Sajjad, Sadegh Biabanifard, Mehdi Hosseini Largani S, et al. DCCII based frequency compensation method for three stage amplifiers. *AEU International Journal of Electronics and Communications*. 2015;69(1):176–181.
18. Largani, Mehdi Hosseini S. A new SMC compensation strategy for three stage amplifiers based on differential feedback path. 22nd Iranian Conference on Electrical Engineering (ICEE); Tehran, Iran: IEEE; 2014.
19. Shahsavari Sajjad, Sadegh Biabanifard, Mehdi Hosseini Largani S et al. A new frequency compensation method based on differential current conveyor. 22nd Iranian Conference on Electrical Engineering (ICEE); May 20–22; Tehran, Iran: IEEE; 2014.
20. Shahsavari Sajjad, Sadegh Biabanifard, Mehdi Hosseini Largani S. Three stages CMOS operational amplifier frequency compensation using single Miller capacitor and differential feedback path. *Analog Integrated Circuits and Signal Processing*. 2018;1–11.
21. Aghaee Toktam, Sadegh Biabanifard, Abbas Golmakani. Gain boosting of recycling folded cascode OTA using positive feedback and introducing new input path. *Analog Integrated Circuits and Signal Processing*. 2017;90(1):237–246.
22. Akbari Meysam, Sadegh Biabanifard, Shahrouz Asadi, et al. Design and analysis of DC gain and transconductance boosted recycling folded cascode OTA. *AEU-International Journal of Electronics and Communications*. 2014;68(11):1047–1052.
23. Akbari Meysam, Sadegh Biabanifard, Shahrouz Asadi, et al. High performance folded cascode OTA using positive feedback and recycling structure. *Analog Integrated Circuits and Signal Processing*. 2015;82(1):217–227.
24. Akbari Meysam, Sadegh Biabanifard, Omid Hashemipour. Design of ultra-low-power CMOS amplifiers based on flicker noise reduction. 22nd Iranian Conference on Electrical Engineering (ICEE); 20-22 May; Tehran, Iran: IEEE; 2014.
25. Akbari Meysam, Sadegh Biabanifard, Shahroz Asadi. Input Referred Noise Reduction Technique for Transconductance Amplifiers. *Electrical & Computer Engineering: An International Journal (ECIJ)*. 2015;4(4):11–22.

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